

# INTELLIGENT INTERACTIVE SYNTHESIZER

## SURFACE MOUNT MODEL: FSWX200800-100

**WIDE BANDWIDTH**

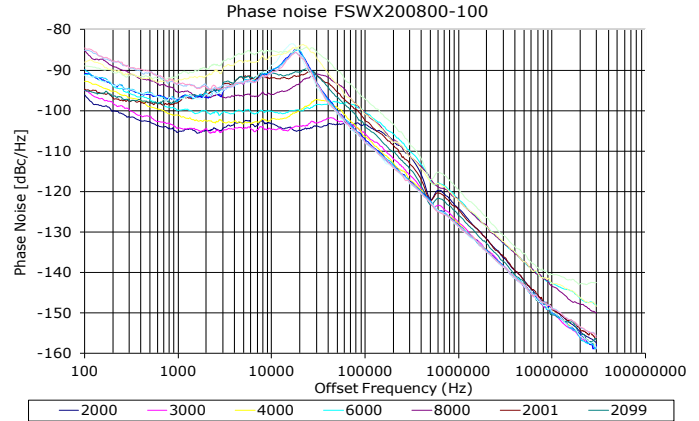
**2000 - 8000 MHz**

**FEATURES:**

- ▶ Exceptionally Low Phase Noise
- ▶ Interactive Communication
- ▶ Standard Programming Interface
- ▶ Ultra Wide Tuning Range
- ▶ Lead Free - RoHS Compliant
- ▶ Patented REL-PRO® Technology
- ▶ Small Size, Surface Mount



**Phase Noise**



**SPECIFICATIONS**

Frequency	2000 - 8000 MHz		
Step Size	1000 kHz		
Reference Input Frequency	100 MHz <sup>1</sup>		
Reference Input Voltage	1.0 V p-p to 3.3 V p-p		
Bias Voltage	<b>Vcc</b>	<b>V (Vdc)</b>	<b>I (mA Max.)</b>
	Digital	+3.3	100
	VCO	+5	200
	Tune	+18	10
Output Power	3 dBm (Typ.)		
Spurious Suppression	57 dB (Typ.)		
Harmonic Suppression	12 dB (Typ.)		
Sub-Harmonic Suppression	15 dB (Typ.)		
Settling Time	10 mSec (Typ.) <sup>2</sup>		
Output Impedance	50 Ohms (Nom.)		
Lock Detect Indicator	CMOS 3.3 V		
Typical Phase Noise (dBc/Hz)	<b>Offset</b>	<b>2 - 4 GHz</b>	<b>4 - 8 GHz</b>
	@ 1 kHz	-100	-95
	@ 10 kHz	-99	-90
	@ 100 kHz	-104	-100
Operating Temperature Range	-40 to +70 °C		
Programming	See Application Note: AN7600		

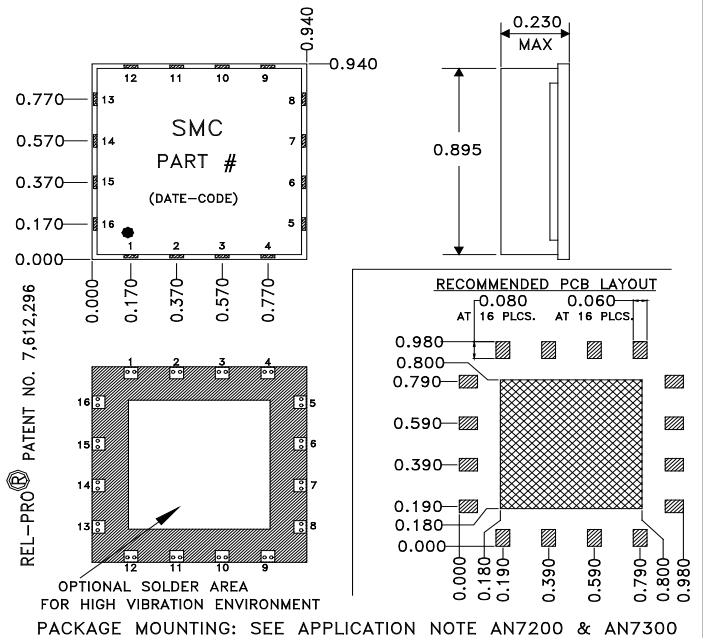
<sup>1</sup> Contact factory if other reference frequency is required.  
<sup>2</sup> From the rising edge of LE to stable lock detect

**Absolute Maximum Ratings**

Storage Temp. Range	-55 to +125 °C
Bias Voltage (Digital)	+3.6 V
Bias Voltage (Tune)	+20 V
Bias Voltage (VCO)	+5.5 V
DC Voltage Applied to RF Out	±25 V

Patent : <http://www.synergymwave.com/patents>

Package # 273LF



**Port Configuration**

Pin 1,2,3,4 - NC	Pin 13 - RF Out	All Others - Ground
Pin 5 - Latch Enable In	Pin 14 - Lock Detect Out *	NC - No Connection
Pin 6 - Ref. In	Pin 15 - Data In	
Pin 7 - Vcc (Digital)	Pin 16 - Clock In	
Pin 8 - Vcc (Tune)		
Pin 9 - Vcc (VCO)		

\* High when locked (source/sink 500 uA)

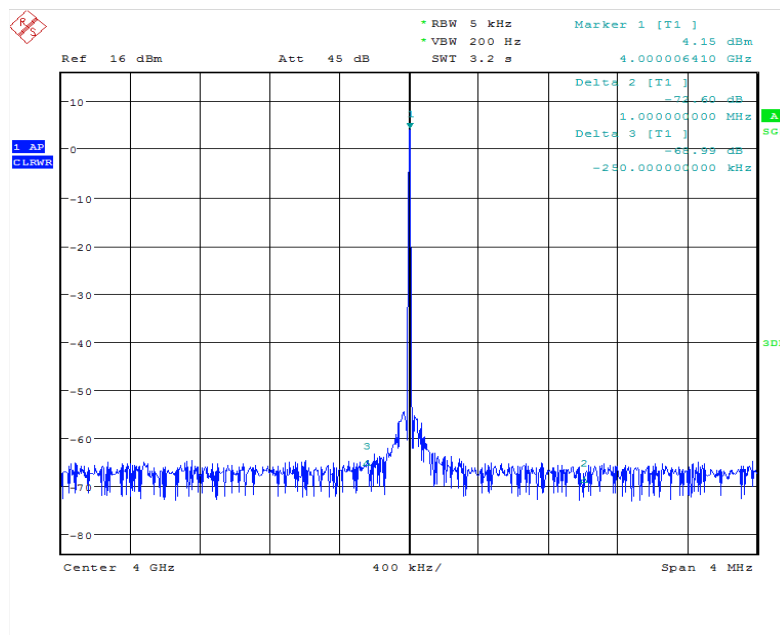
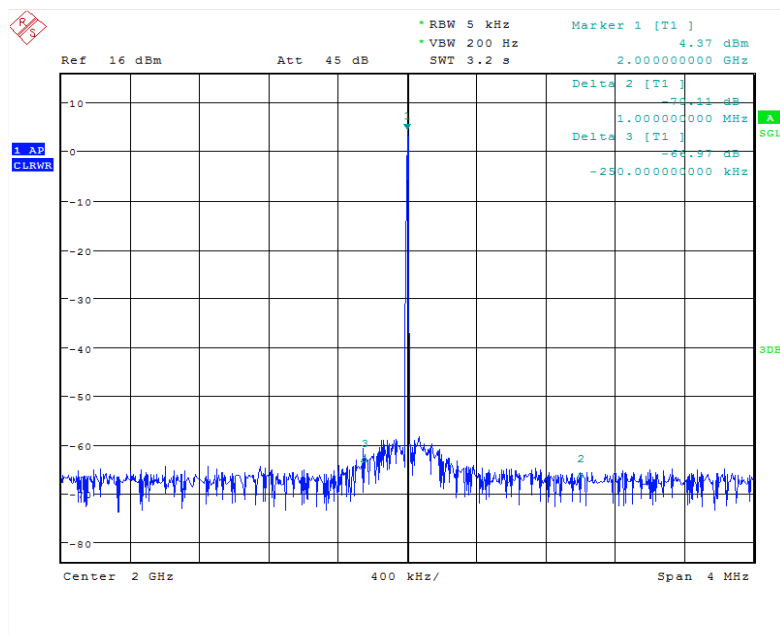
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### SPURIOUS MEASUREMENT



PERFORMANCE PLOTS

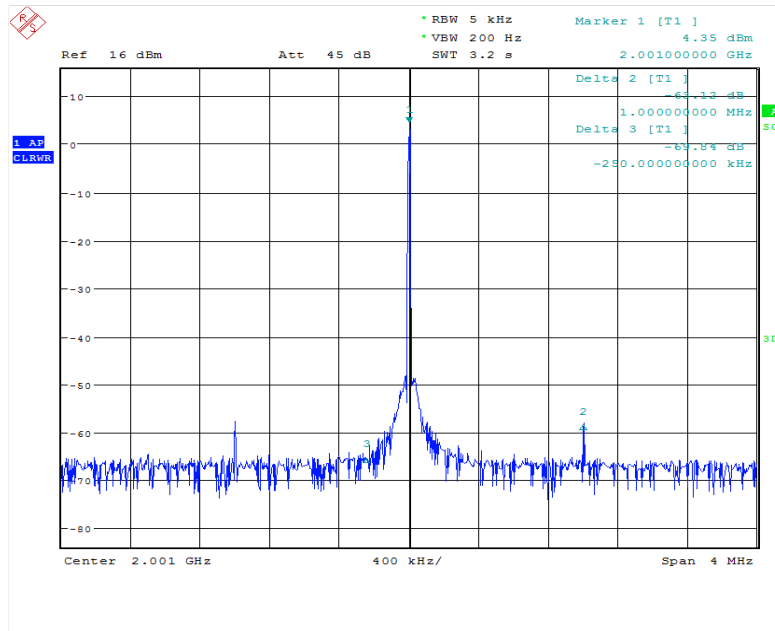
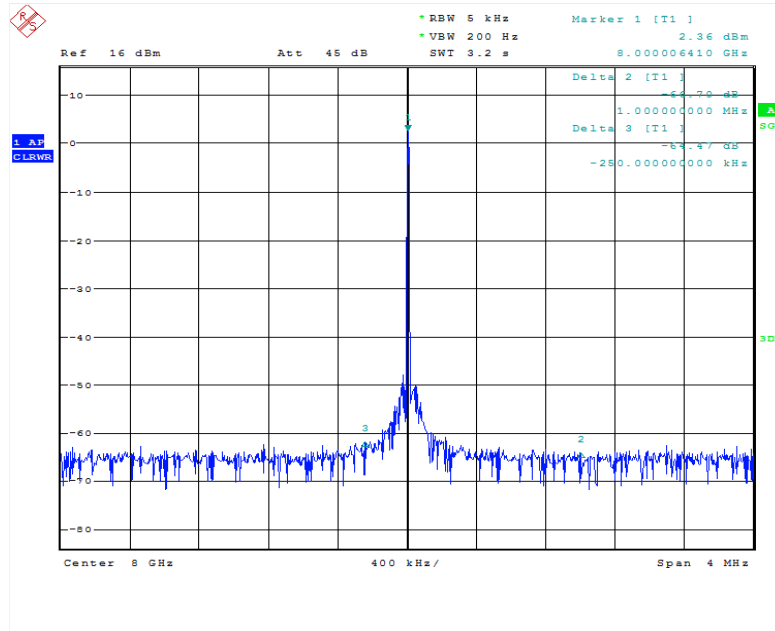
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PERFORMANCE PLOTS

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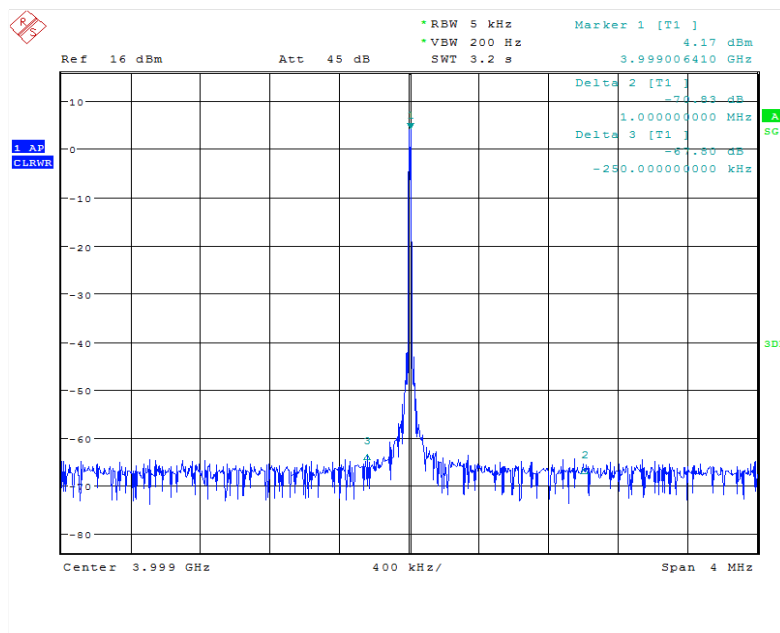
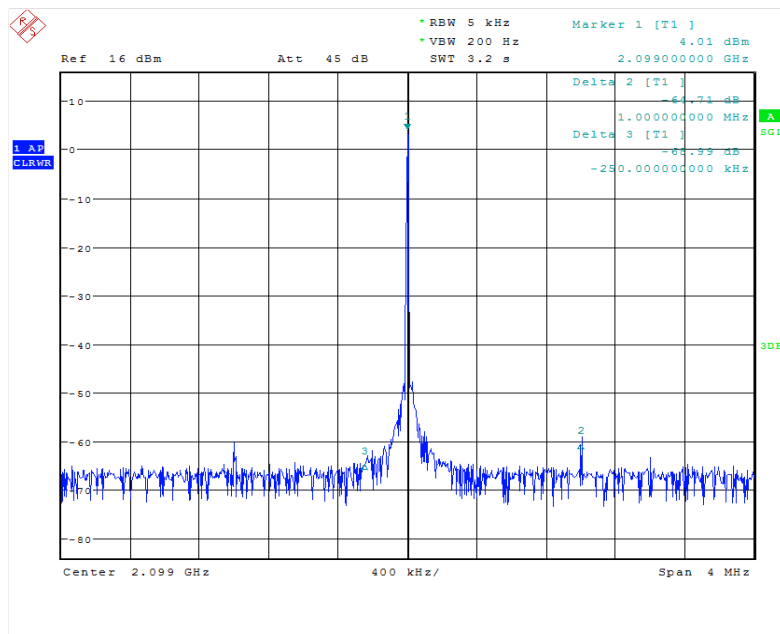
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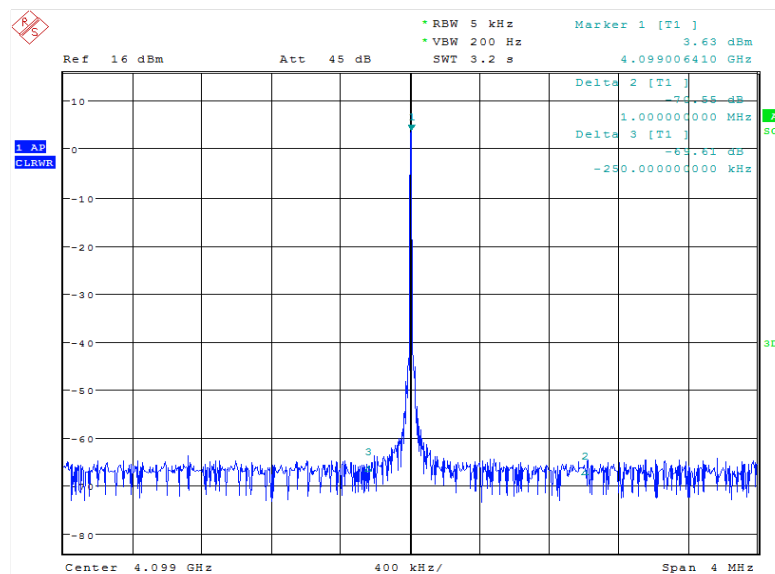
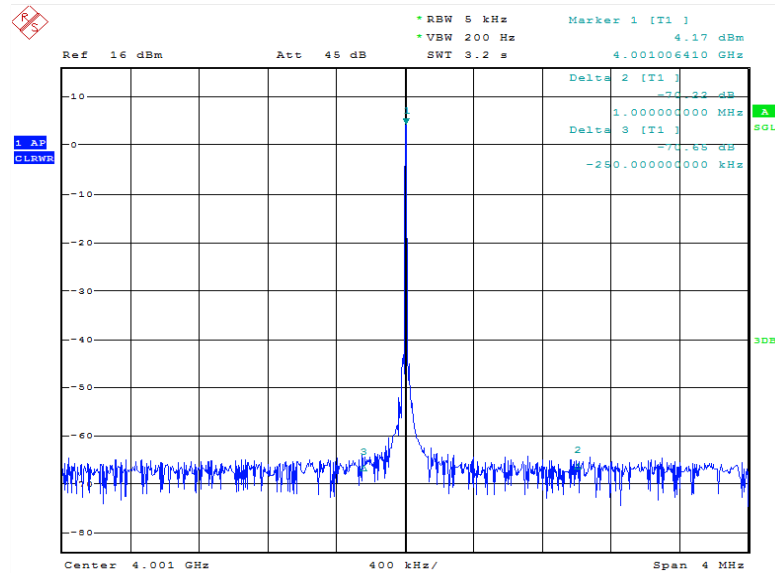
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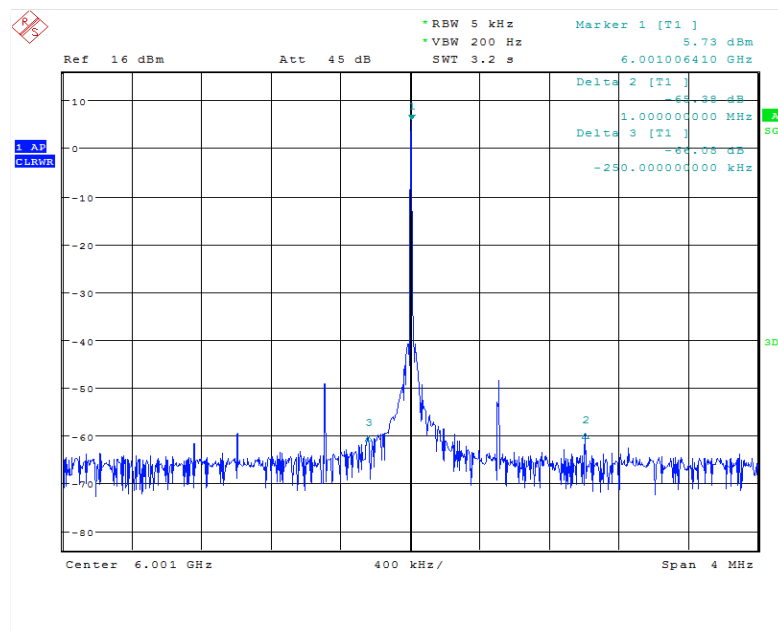
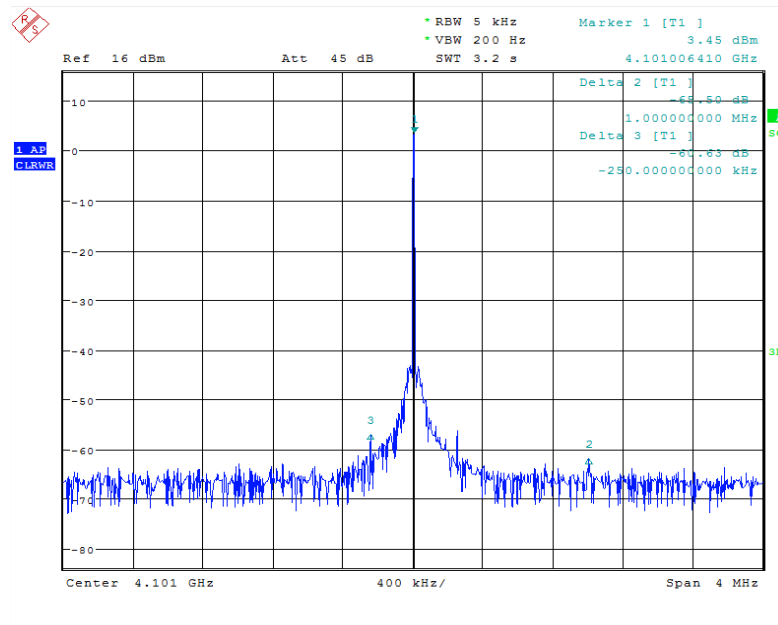
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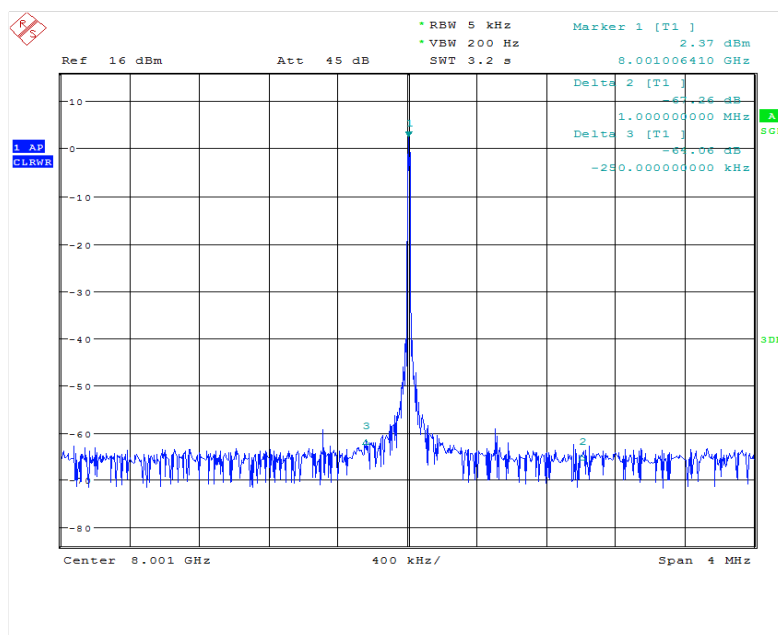
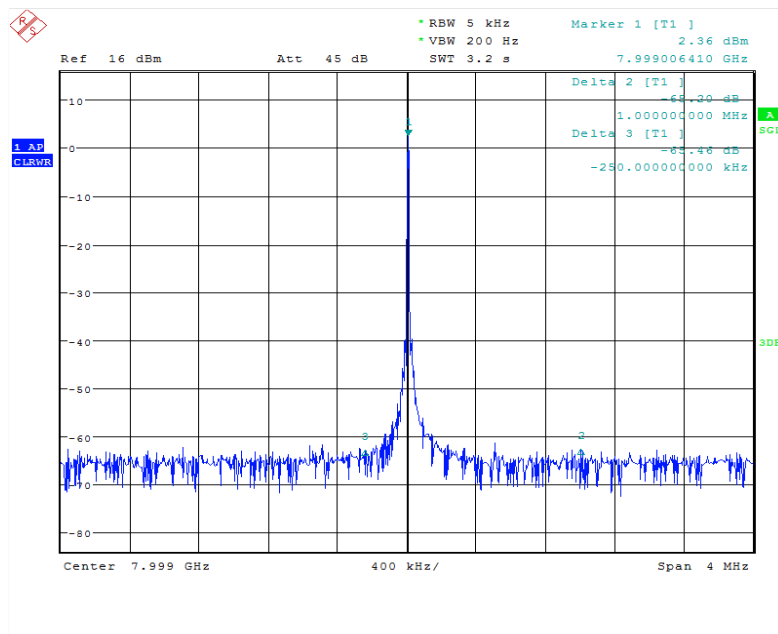
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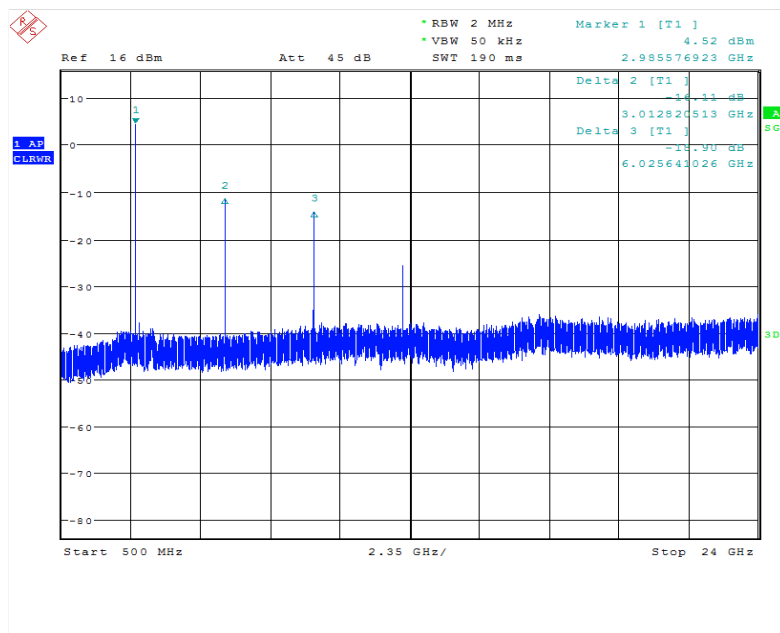
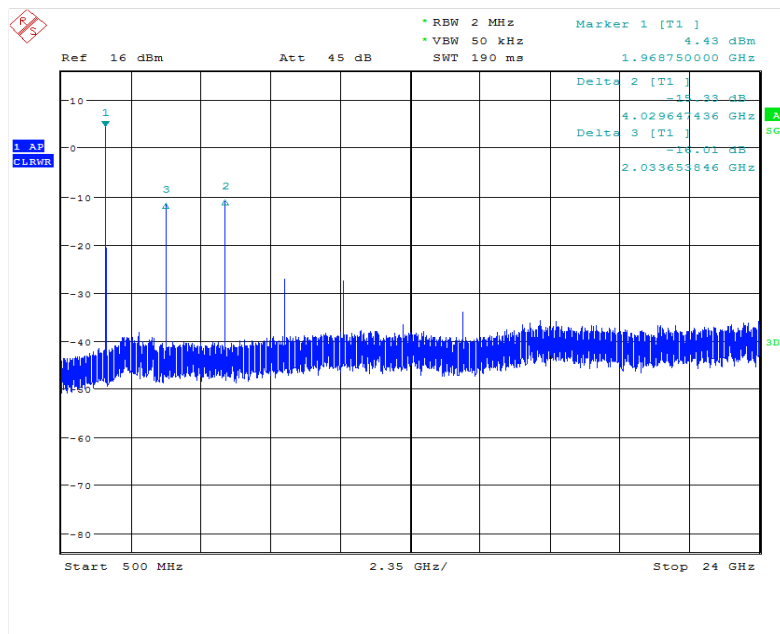
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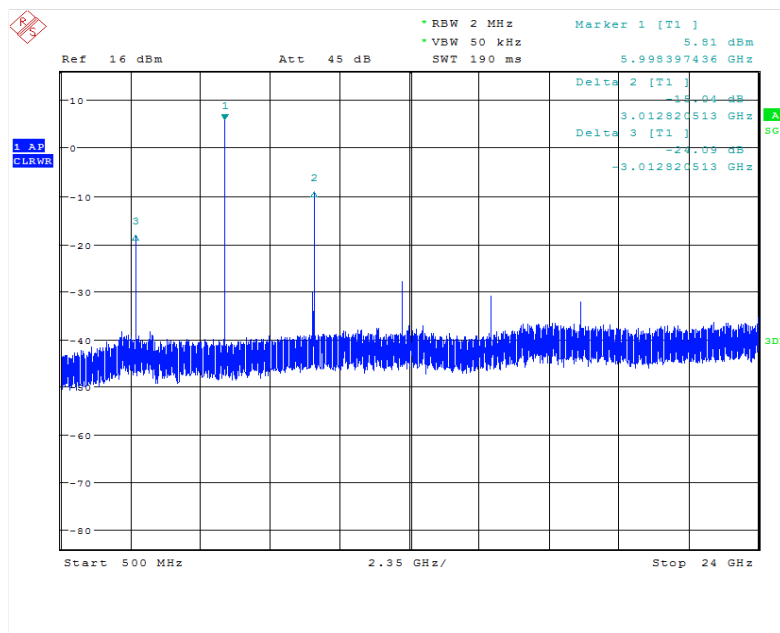
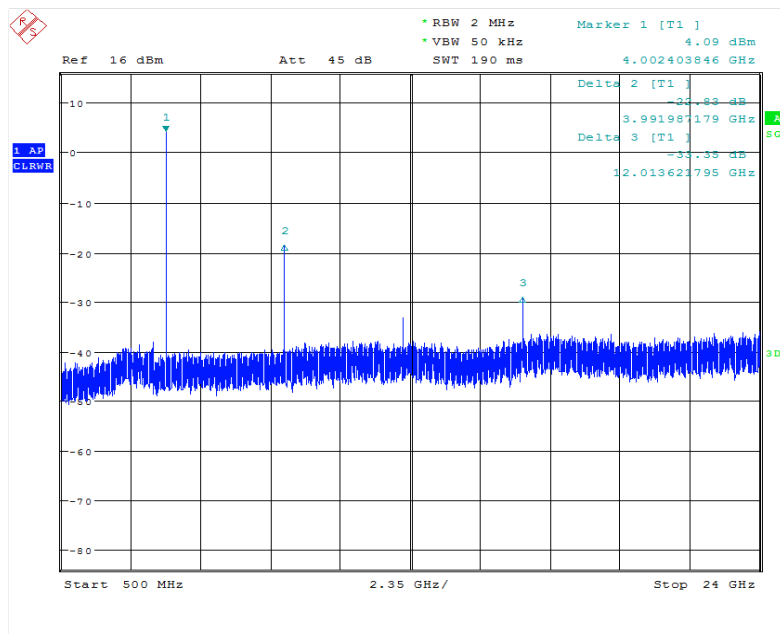
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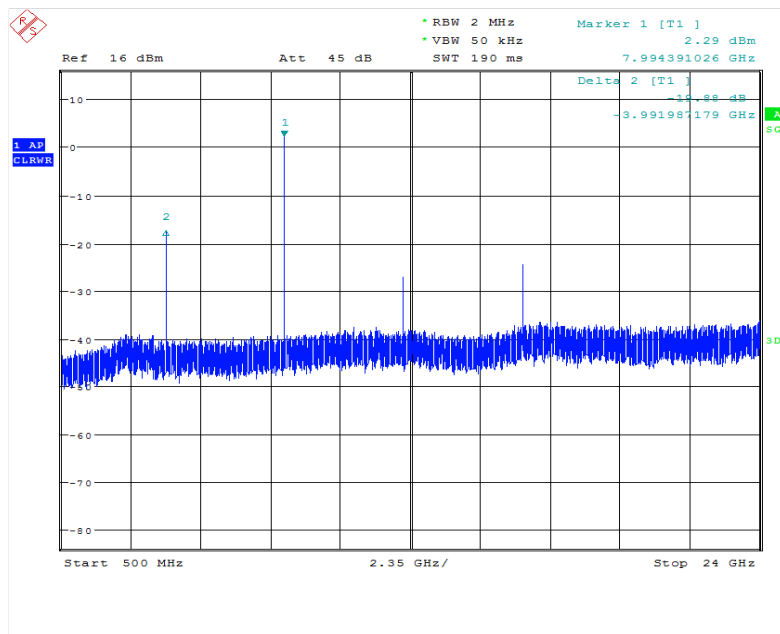
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