

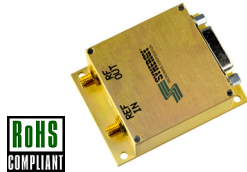
PARALLEL ADDRESSABLE SYNTHESIZER CONNECTORIZED MODEL: KFCPL65120-10

SELECTABLE FREQUENCY

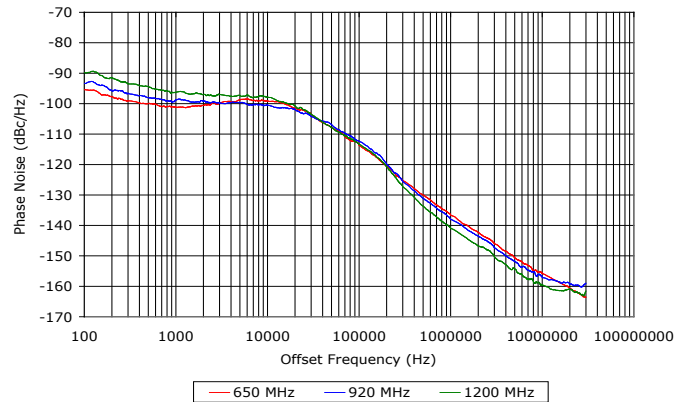
650 - 1200 MHz

FEATURES:

- ▶ Exceptional Phase Noise
- ▶ No Programming Required
- ▶ Lead Free - RoHS Compliant
- ▶ Up to 16 selectable frequencies
- ▶ Buffered Output



Phase Noise



SPECIFICATIONS (Rev. J 11/15/23)

Frequency	650 - 1200 MHz		
Reference Input Frequency	10 MHz		
Reference Input Voltage	1.0 V p-p to 3.3 V p-p		
Bias Voltage	Vcc	V (Vdc)	I (mA Max.)
	Vcc 1 (Digital)	+5	15
	Vcc 2 (Vtune)	+12	10
	Vcc 3 (VCO)	+5	58
Output Power	+6 dBm (Min.)		
Spurious Suppression	100 dB (Typ.)		
Harmonic Suppression	15 dB (Typ.)		
Power Up Time	90 mSec (Max.) ¹		
Output Impedance	50 Ohms (Nom.)		
Typical Phase Noise	Offset	Phase Noise	
	@ 10 kHz	-98 dBc/Hz	
	@ 100 kHz	-113 dBc/Hz	
Lock Detect Indicator	CMOS 3.3 V		
Operating Temperature Range	-40 to +85 °C		

¹ From stable power on to stable lock detect.

Binary Frequency Selection Table

D3	D2	D1	D0	Freq. (MHz)
0	0	0	0	790
0	0	0	1	860
0	0	1	0	1010
0	0	1	1	915
0	1	0	0	920
0	1	0	1	1090
0	1	1	0	800
0	1	1	1	725
1	0	0	0	700
1	0	0	1	750
1	0	1	0	950
1	0	1	1	--
1	1	0	0	--
1	1	0	1	--
1	1	1	0	--
1	1	1	1	--

-- Reserved for future use.

* Voltage levels: 0V or gnd. / +5V or open.

Absolute Maximum Ratings

Storage Temp. Range	-55 to +125 °C
Bias Voltage (Digital)	+5.25 V
Bias Voltage (VCO)	+26 V
DC Voltage Applied to RF Out	± 25 V

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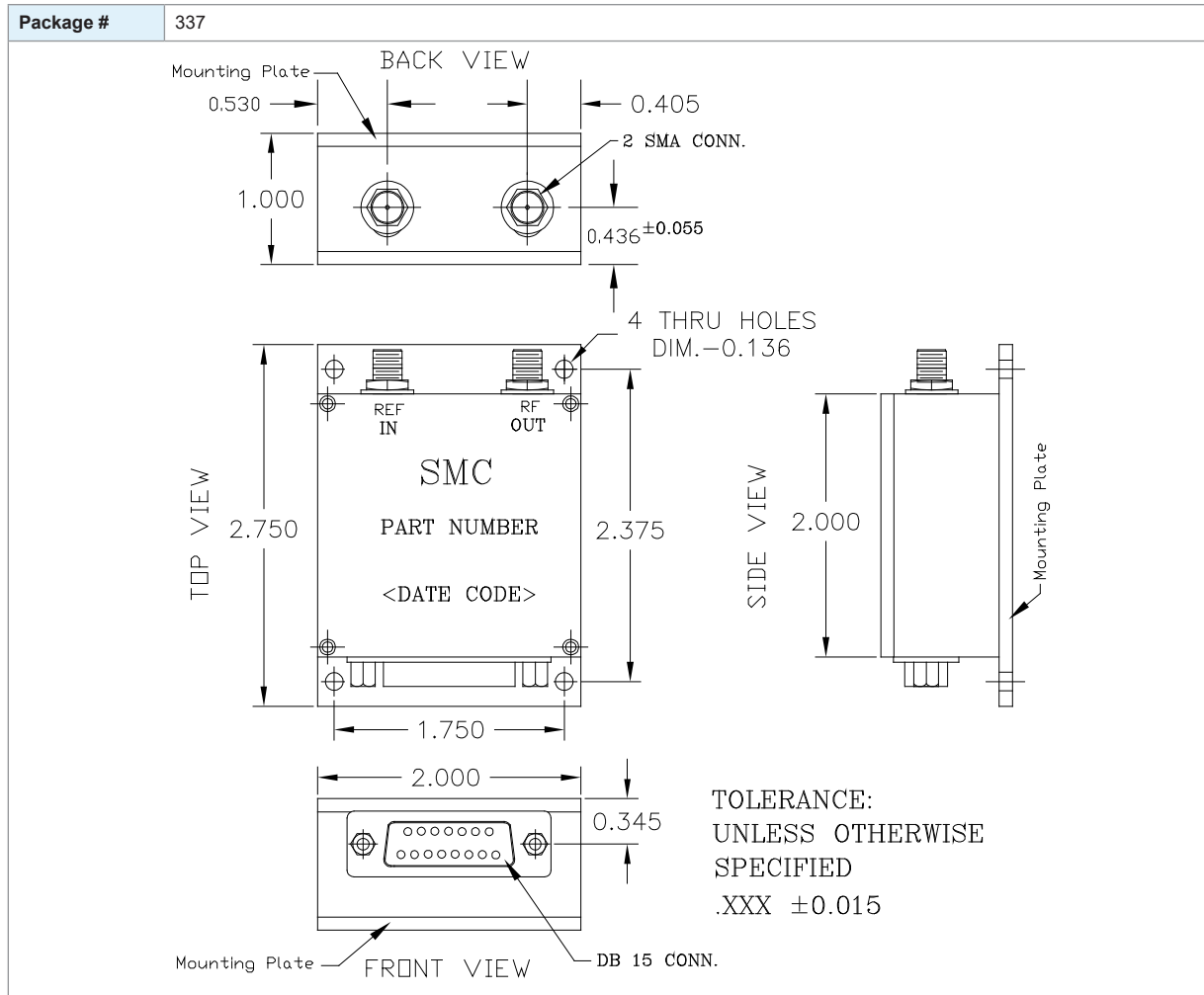


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PERFORMANCE PLOTS



Port Configuration

Pin 1 - VCC1 (Digital)	Pin 5 - NC	Pin 9 - VCC3 (VCO)	Pin 13 - D2
Pin 2 - VCC2 (Vtune)	Pin 6 - NC	Pin 10 - Ground	Pin 14 - D3
Pin 3 - NC	Pin 7 - NC	Pin 11 - D0	Pin 15 - Ground
Pin 4 - NC	Pin 8 - Lock Detect	Pin 12 - D1	

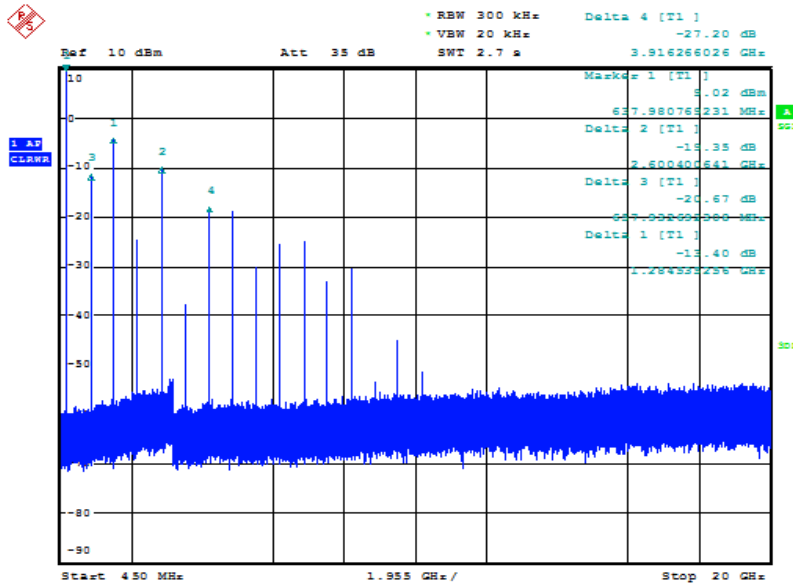
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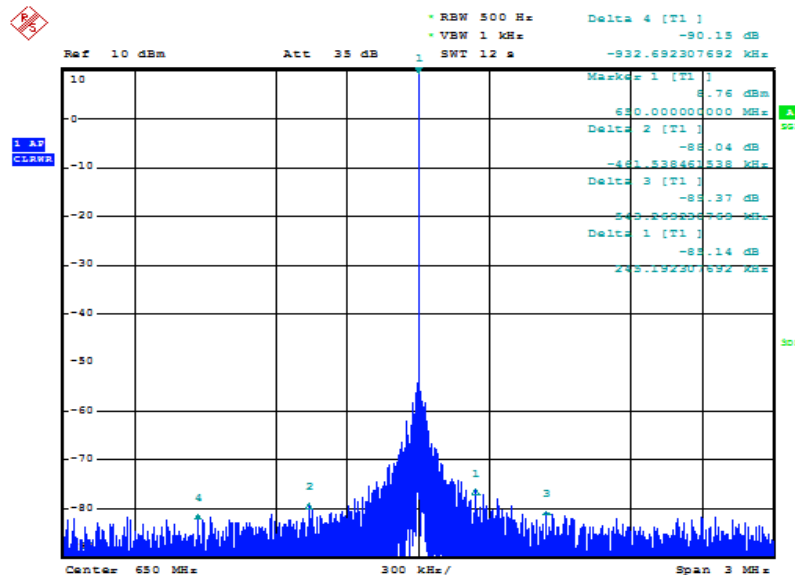
650 - 1200 MHz

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HARMONIC SUPPRESSION



REFERENCE SIDEBAND SUPPRESSION



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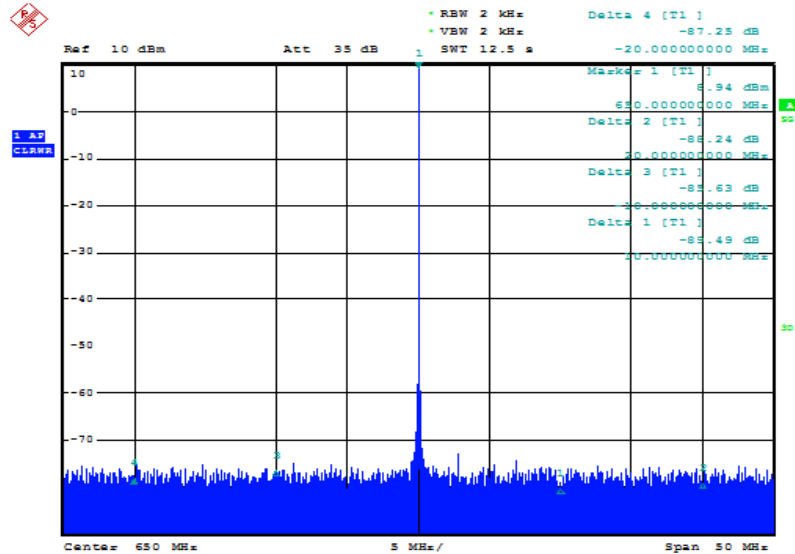


PARALLEL ADDRESSABLE SYNTHESIZER CONNECTORIZED MODEL: KFCPL65120-10

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CLOSE IN SPURIOUS SUPPRESSION



PERFORMANCE PLOTS

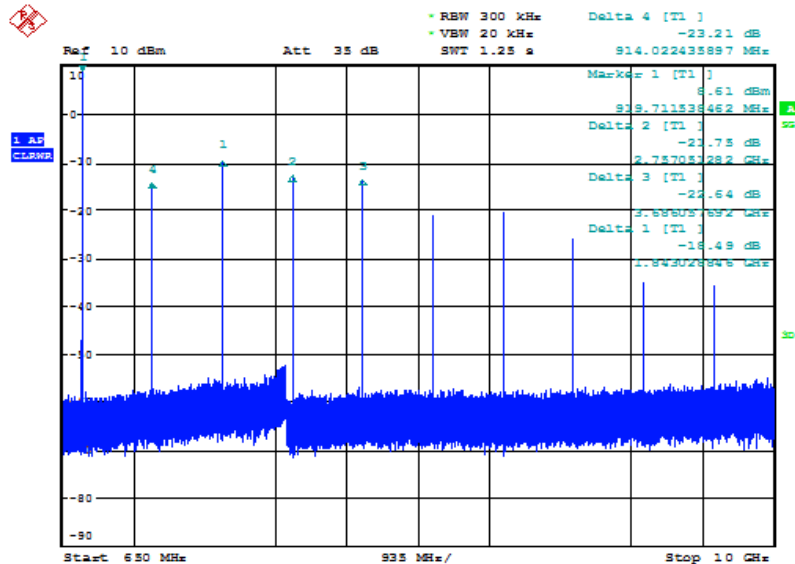
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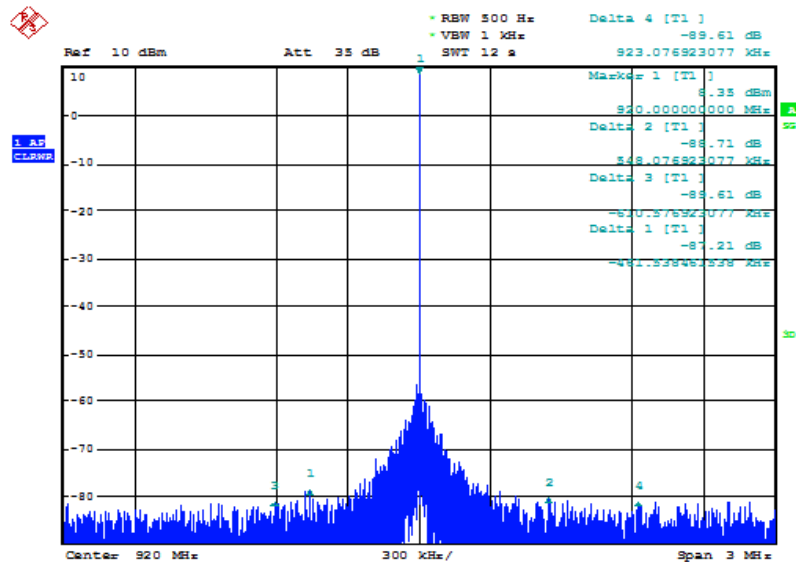
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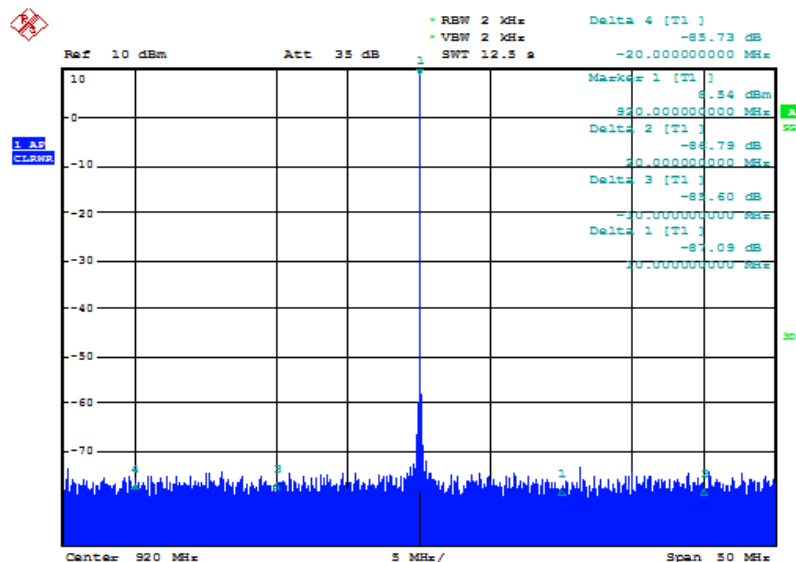


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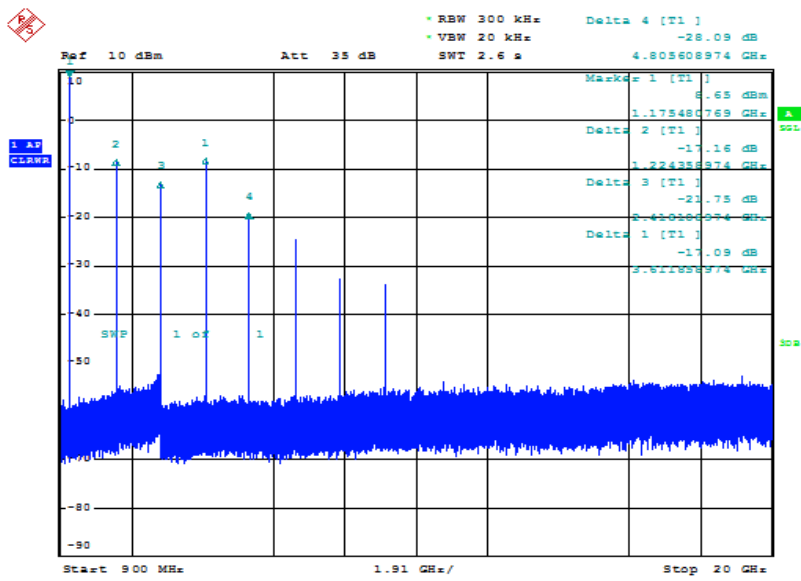
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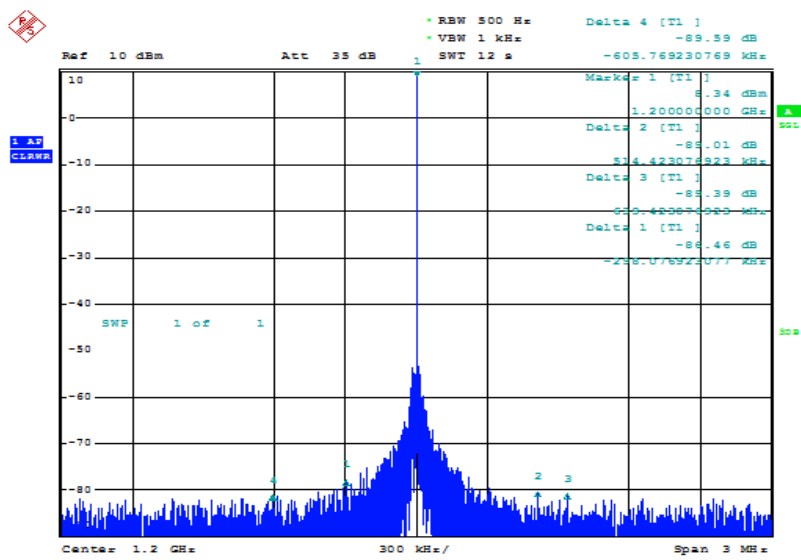
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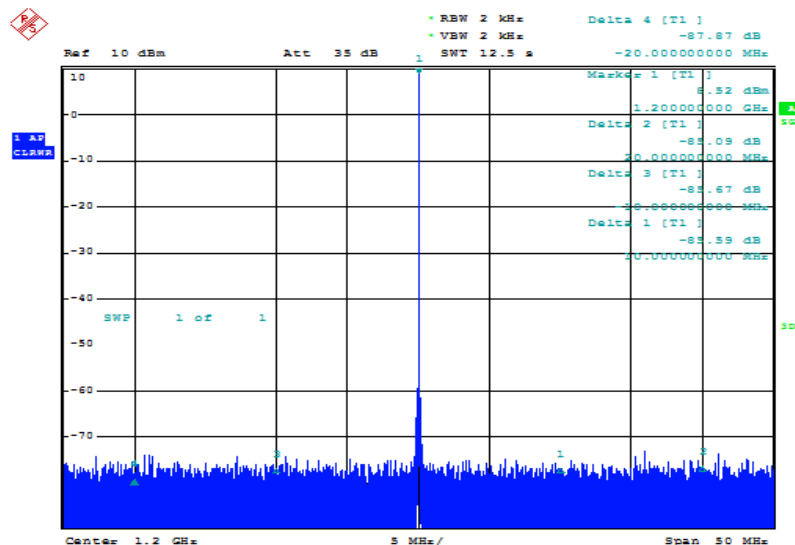


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