

# REFERENCE PHASE LOCKED TRANSLATOR

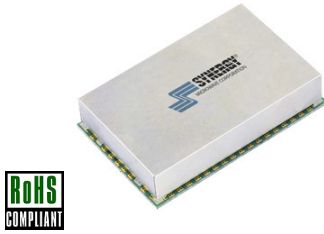
## SURFACE MOUNT MODEL: FSA1000-100

**FIXED FREQUENCY**

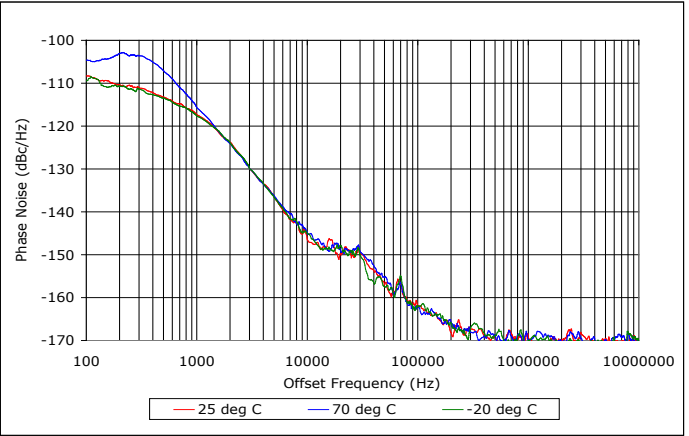
**1000 MHz**

**FEATURES:**

- ▶ Ultra-Low Phase Noise
- ▶ No Programming Required



Phase Noise ( Measured with Agilent E5052A or R&S FSUP-26/50 )



**SPECIFICATIONS**

Frequency	1000 MHz																		
Reference Input Frequency	100 MHz <sup>1</sup>																		
Reference Input Voltage	1.0 to 3.3 V p-p																		
Bias Voltage	<table border="1"> <thead> <tr> <th>VCC</th> <th>VDC @ I</th> </tr> </thead> <tbody> <tr> <td>1 (RF)</td> <td>+5 VDC @ 50 mA (Max.)</td> </tr> <tr> <td>2 (Analog)</td> <td>+3.3 VDC @ 10 mA (Max.)</td> </tr> <tr> <td>3 (RF, 1 GHz)</td> <td>+3.3 VDC @ 50 mA (Max.)</td> </tr> <tr> <td>4 (Reference)</td> <td>+5 VDC @ 150 mA (Max.)</td> </tr> <tr> <td>5 (Vtune)</td> <td>+12 VDC @ 20 mA (Max.)</td> </tr> <tr> <td>6 (PLL)</td> <td>+5 VDC @ 10 mA (Max.)</td> </tr> <tr> <td>7 (PLL)</td> <td>+3.3 VDC @ 10 mA (Max.)</td> </tr> <tr> <td>8 (VCO)</td> <td>+5 VDC @ 50 mA (Max.)</td> </tr> </tbody> </table>	VCC	VDC @ I	1 (RF)	+5 VDC @ 50 mA (Max.)	2 (Analog)	+3.3 VDC @ 10 mA (Max.)	3 (RF, 1 GHz)	+3.3 VDC @ 50 mA (Max.)	4 (Reference)	+5 VDC @ 150 mA (Max.)	5 (Vtune)	+12 VDC @ 20 mA (Max.)	6 (PLL)	+5 VDC @ 10 mA (Max.)	7 (PLL)	+3.3 VDC @ 10 mA (Max.)	8 (VCO)	+5 VDC @ 50 mA (Max.)
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Output Power	+5 dBm (Min.)																		
Spurious Suppression	80 dB (Typ.)																		
Harmonic Suppression	15 dB (Typ.)																		
Output Impedance	50 Ohms (Nom.)																		
Lock Detect Indicator	CMOS 3.3 V																		
<sup>1</sup> External 100 MHz reference sources should have phase noise better than -138 dBc/Hz @ 50 Hz offset to achieve published specifications.																			

Typical Phase Noise	<table border="1"> <thead> <tr> <th>Offset</th> <th>Phase Noise</th> </tr> </thead> <tbody> <tr> <td>@ 100 Hz</td> <td>-105 dBc/Hz</td> </tr> <tr> <td>@ 1 kHz</td> <td>-115 dBc/Hz</td> </tr> <tr> <td>@ 10 kHz</td> <td>-145 dBc/Hz</td> </tr> <tr> <td>@ 100 kHz</td> <td>-160 dBc/Hz</td> </tr> </tbody> </table>	Offset	Phase Noise	@ 100 Hz	-105 dBc/Hz	@ 1 kHz	-115 dBc/Hz	@ 10 kHz	-145 dBc/Hz	@ 100 kHz	-160 dBc/Hz
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	@ 100 Hz	-105 dBc/Hz									
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Operating Temperature Range	-20 to +70 °C										

**Absolute Maximum Ratings**

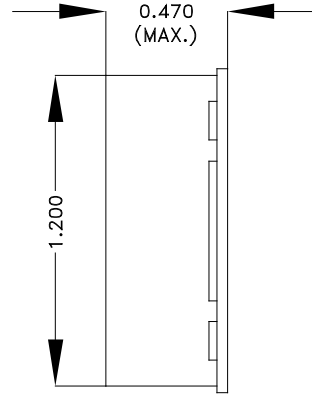
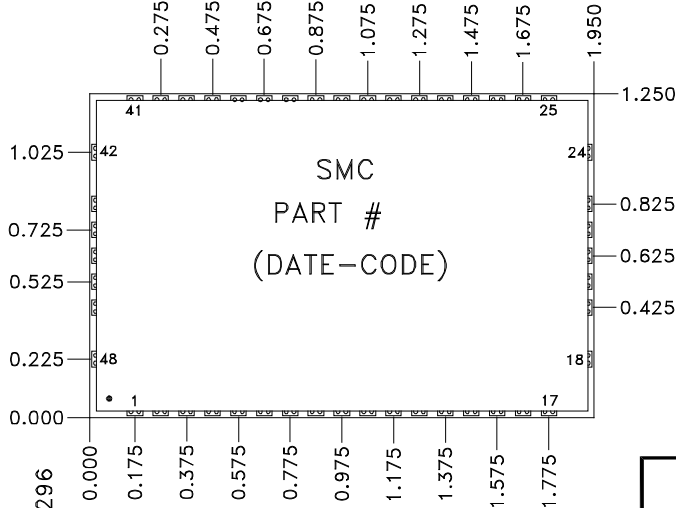
Storage Temp. Range	-40 to +85 °C
Bias Voltage (+3.3 V)	+3.6 V
Bias Voltage (+5 V)	+5.5 V
DC Bias Voltage applied to RF output	±25 V
Bias Voltage (+12 V)	+14 V

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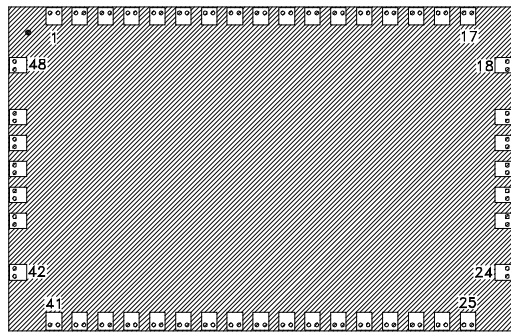
FIXED FREQUENCY

1000 MHz

Package # 344



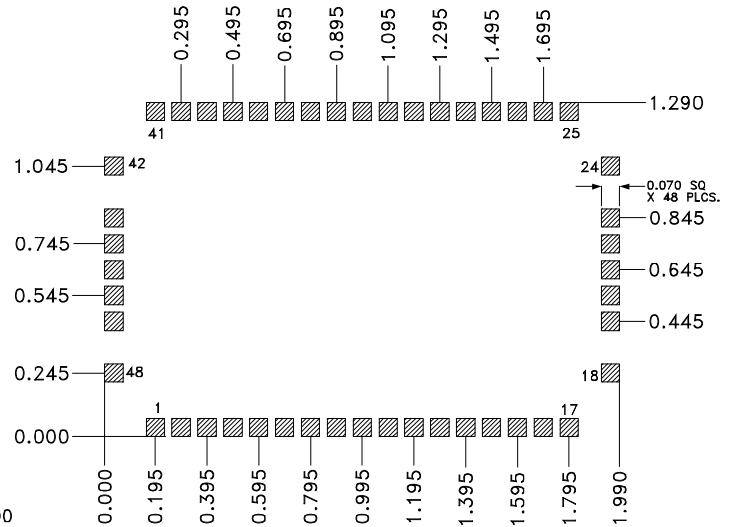
REL-PRO PATENT NO. 7,612,296



TOLERANCES ON THREE  
DECIMAL PLACES =  $\pm 0.015$

PACKAGE MOUNTING: SEE APPLICATION NOTE AN7200 & AN7300

## RECOMMENDED PCB LAYOUT



## PORT CONFIGURATION

Pin 3 - VCC 1 (VCC RF)  
Pin 6 - RF OUT  
Pin 8 - VCC 2 (Analog = +3.3 VDC)  
Pin 9 - NC  
Pin 10 - NC  
Pin 11 - VCC 3 (Digital = +3.3 VDC)  
Pin 12 - NC  
Pin 13 - NC  
Pin 14 - Lock Detect (LD) \*\*  
Pin 15, 16 - NC

Pin 18,19,20,21 - NC  
Pin 22 - Reference In  
Pin 27 - VCC 4 (Reference = +5 VDC)  
Pin 28 - VCC 5 (Vtune = +12 VDC)\*  
Pin 30,31 - NC  
Pin 35 - NC  
Pin 39 - VCC 6 (PLL = +5 VDC)  
Pin 40 - VCC 7 (PLL = +3.3 VDC)  
Pin 44 - VCC 8 (VCO = +12 VDC)\*  
Pin 43,45 - NC

All others - Ground  
1,2,4,5,7,17,23-26,32-34,36-38,41,42,46-48

NC - No connection

\* Connect together externally and bypass with shunt 10  $\mu$ F, 35 V capacitor to ground.  
\*\* Positive CMOS levels (unbuffered 3.3 VDC)

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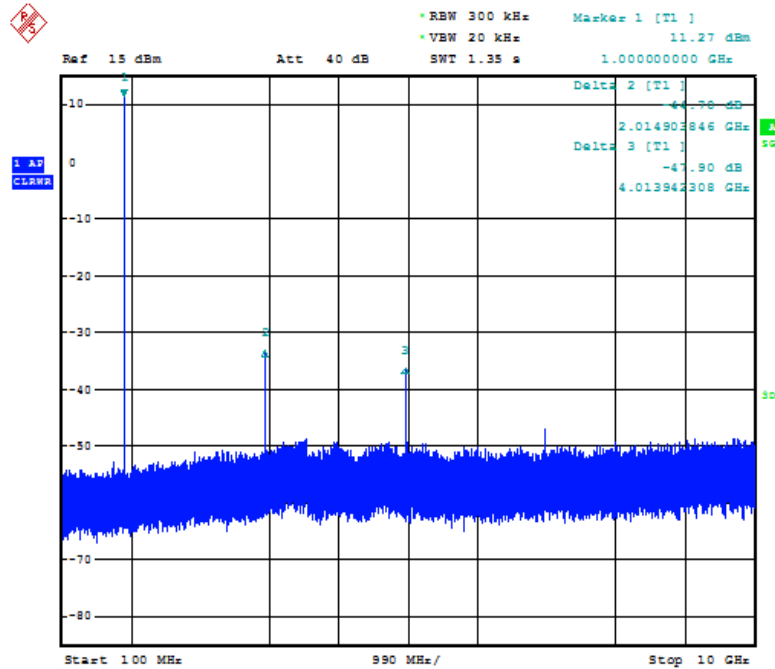
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1000 MHz

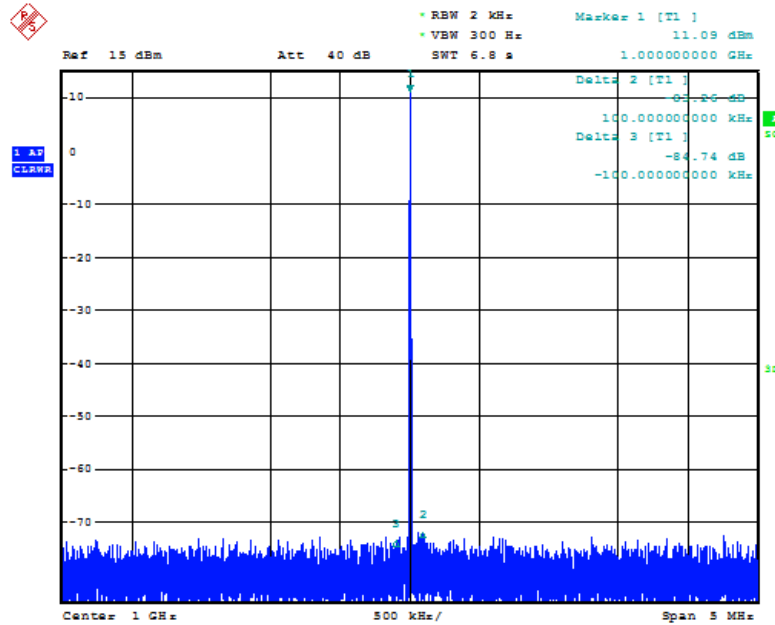
@ 25 °C

PERFORMANCE PLOTS

HARMONIC SUPPRESSION



REFERENCE SIDEBAND SUPPRESSION



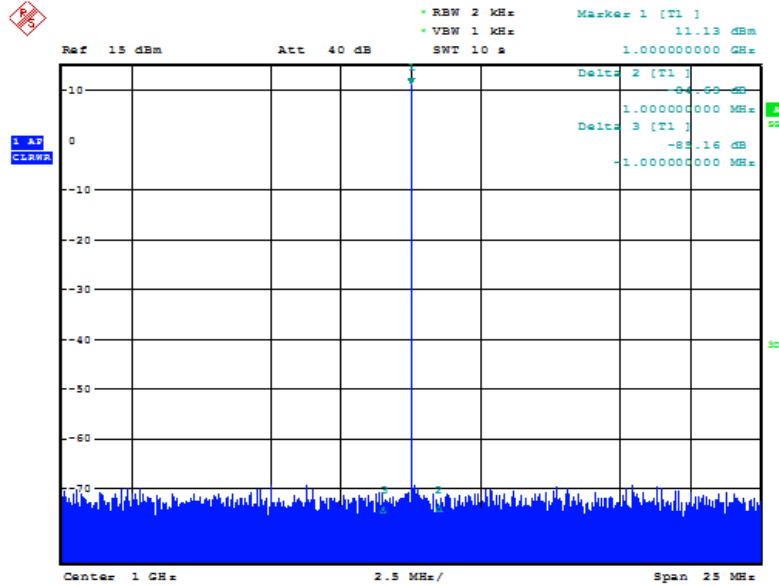
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