Cover Story

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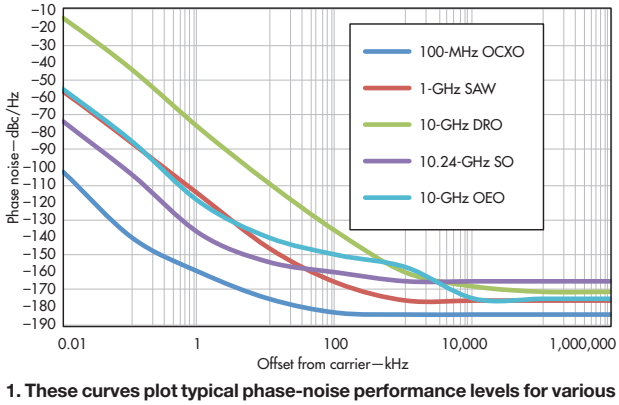
Searching For Low-Phase

A hybrid approach shows great promise in achieving frequency synthesized microwave signals with low phase both close to and far from the carrier.

Clean, quiet frequency synthesizers are essential for modern communications systems. But the performance of RF/microwave frequency synthesizers is often tied to a lower-frequency reference oscillator, such as an oven-controlled crystal oscillator (OCXO), and great effort is often required to produce a microwave frequency synthesizer with low phase noise. To demonstrate, a 10.24-GHz frequency synthesizer with OCXO reference source was developed, and the design path to that synthesizer will be traced.

Phase noise is a vital parameter for oscillators and synthesizers in communications and other systems. It is measured as the ratio between the power density in one phase noise modulation sideband, per hertz, and total signal power.[1] Typically, a wideband synthesizer will exhibit more noise than a single-frequency synthesizer. When low noise is required, a single-frequency synthesizer can be combined with frequency mixers to build a wideband synthesizer with low noise.

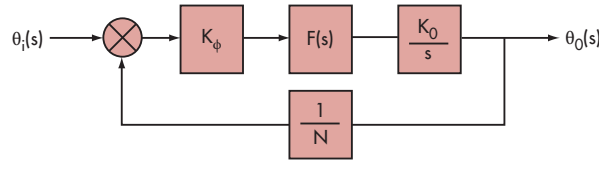
The phase noise of the signal produced by the synthesizer is determined by the performance of the oscillator used to build the synthesizer, the performance of the reference, and the transfer characteristic and intrinsic noise of the synchronization method. Major contributors to phase noise are the internal oscillator and the reference source (for noise offset far from and close to the carrier, respectively). An OCXO may be used as the reference for low-noise applications, possibly locked to a rubidium clock or a 1-pulse-per-second GPS source.



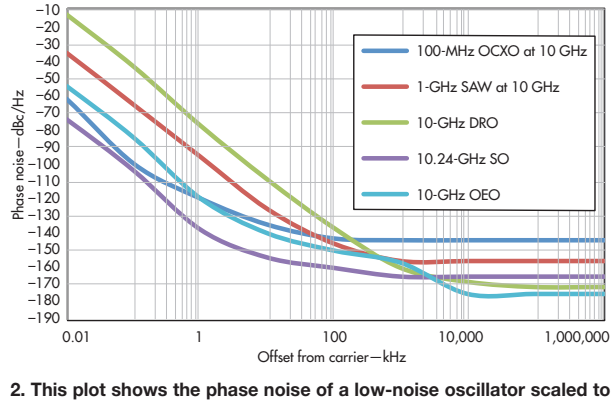
1. These curves plot typical phase-noise performance levels for various low-noise oscillators.

The phase noise performance of the oscillators has a fundamental limit imposed by the Johnson-Nyquist theory. A resistor at room temperature (300 K) produces about −173.82-dBm/Hz noise, with this power level equally split in two sidebands. A signal with 0-dBm power will have a lower phase-noise limit of −177 dBc/Hz, improving upon −177 dBc/Hz only if the signal carries more than 0-dBm power, as with some low-noise OXCOs.[2,3] The best low-noise oscillators are capable of approaching this limit at far offset frequencies. For close-in frequency offsets the phase noise will be determined by the quality factor (Q) of the resonator.

The frequency offset at which the phase noise approaches the theoretical limit is roughly proportional to the frequency of the oscillator, increasing as the frequency increases. *Figure 1* shows typical performance levels for different low-noise oscillators, including a 100-MHz OCXO, a 1-GHz surface-acoustic-wave (SAW) oscillator, a 10-GHz dielectric-resonator oscillator (DRO), a 10.24-GHz sapphire oscillator (SO), and a 10-GHz opto-electronic oscillator (OEO).[4-10]



3. This block diagram represents a second-order phase-locked loop (PLL) for low-noise frequency synthesis.



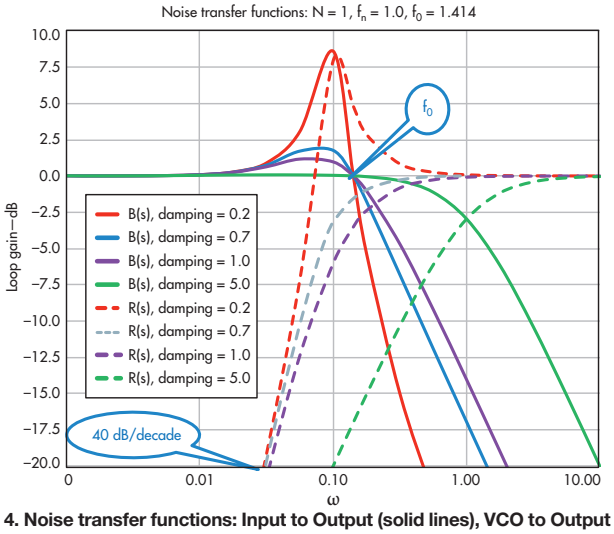
2. This plot shows the phase noise of a low-noise oscillator scaled to a 10-GHz output frequency.

In *Fig. 1*, the OCXO phase noise exceeds the –177-dBc limit, because its power is 13 dB higher than the 0-dBm limit. The lowest-frequency oscillators typically exhibit the lowest noise floors. They also show lower close-in phase noise, since the quality factor (Q) of lower-frequency resonators is higher, and because the flicker characteristics associated with these resonators is better. When using these oscillators as the reference of a synthesizer, their noise contribution is scaled by $20\log(F_{out}/F_{ref})$. Thus, the noise contribution of a 100-MHz OCXO will be increased by 40 dB when producing a 10-GHz signal. *Figure 2* shows the expected noise from these oscillators when used to generate a 10-GHz signal.

The lowest close-in phase noise is from the sapphire oscillator (SO), followed closely by the OCXO. The lowest phase noise far from the carrier is for the optoelectronic oscillator (OEO) and the dielectric-resonator oscillator (DRO). Combining the SO or OCXO with the OEO or DRO could achieve lower noise levels. (Additional specifications are available in *Table 1* at www.mwrf.com/active-components/searching-low-phase-noise-synthesizers.)

TABLE 1: TYPICAL PERFORMANCE SPECIFICATIONS FOR DIFFERENT OSCILLATORS

Parameter	OCXO	SAW	DRO	Sapphire	OEO
Size (in.)^3	1.5 × 1.1 × 0.7	0.5 × 0.5 × 0.2	1.3 × 3.1 × 0.8	8.5 × 8.5 × 2.5	4.5 × 5.9 × 0.94
Weight	0.9 oz.	0.1 oz.	0.2 lb.	15.5 lb.	--
Power consumption (W)	1.5	0.175	5	34.5	28
Cost	Moderate	Low	Moderate	Very high	--
Operating temperature range (°C)	–20 to +60	–20 to +70	–15 to +75	0 to +50	+15 to +45
Output power (dBm)	+15	+2	8dBm	>10dBm	>10dBm
Harmonics (dBc)	–40	–25	–40	--	–40
Spurious (dBc)	--	--	--	–130	–95



4. Noise transfer functions: Input to Output (solid lines), VCO to Output (dashed lines).

Figure 3 shows a typical second-order PLL circuit that can be used as the starting point for building a frequency synthesizer. It uses a phase detector, loop filter, oscillator, and feedback divider.[10-12] Parameter K_φ is the gain of the phase detector, F(s) is the transfer characteristic of the loop filter, K_0 is the VCO sensitivity, and N is the feedback divider ratio. Considering the PLL a control system, the closed-loop transfer function (transfer function of the input phase noise to the output signal) can be described by Eq. 1:

$$B(s) = \varphi_0(s)/\varphi_i(s) = N[(2\xi\omega_n s + \omega^2{}_n/(s^2 + 2\xi\omega_n s + \omega^2{}_n] \quad (1)$$

with F(s), the natural pulsation (ω_n), and the damping factor of the control system (ξ) described by Eqs. 2, 3, and 4, respectively:

$$F(s) = (1 + \tau_2 s)/(\tau_1 s) \quad (2)$$

$$\omega_n = [\, K_\varphi K_0/(N\tau_2)]^{0.5} \quad (3)$$

$$\xi = \omega_n \tau_2/2 \quad (4)$$

By analyzing Eq. 1, as the input phase-noise frequency offset decreases towards zero, the transfer function approaches N. The feedback divider ratio amplifies the input phase noise, increasing by a factor of 20logN (in dBc). The unity gain frequency (f_0) is independent on the damping factor and is given by Eq. 5[13]:

$f_0 = [(2)^{0.5}/2\pi]\rho_n$ (5)

The VCO noise transfers to the output of the PLL by a second-order highpass relationship given by Eq. 6:

$R(s) = s^2/(s^2 + 2\xi\omega_n s + \omega^2_n)$ (6)

For low offset frequencies, the VCO noise is attenuated with a 40-dB/decade slope, while for far offset frequencies, the VCO noise passing to the output is unaffected by the loop.

The magnitudes of the B(s) and K(s) noise transfer functions are plotted in *Fig. 4*. For a damping factor of 0.707, shown by the blue trace on *Fig. 4*, the peaking has a value of 2.09 dB. If the PLL is underdamped ($\xi < 0.707$), peaking can be large, making the system unstable. Peaking can be reduced by increasing the damping factor, but this takes the B(s) and R(s) trace decrease less sharply beyond the natural frequency.

TABLE 2: COMPARING THE THREE PHASE-NOISE MODELS

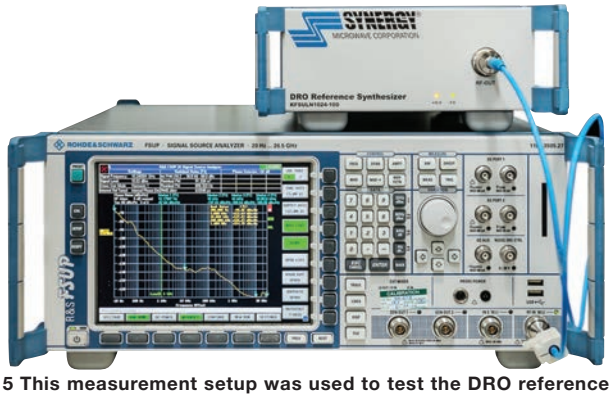
Model	Leeson	Lee and Hajimiri	Kaertner and Demir
Assumptions	LTIV	LTV	NLTV
Perturbing noise source	Constant white noise (kTB)	Cyclostationary 1/fk for any k that is an element of N	Modulated 1/fk for any k that is an element of N
Accuracy	Reasonable	Good	Exact
Simplicity	Simple	Moderate	Involved
Computer dependence	Independent (Calculation by hand)	Computer to evaluate ISF	Computer dependent (no closed form solutions)
Predicts close-in phase noise	No	Yes	Yes
Retained circuit parameters	Loaded Q-factor (QL), output power (Ps)	Q_{max}	None

Noise models can be categorized as linear time invariant (LTIV), linear time variant (LTV), and nonlinear time variant (NLTV) models, in order of increasing complexity. Leeson's model[15] is based on LTIV oscillator properties, such as resonator Q, feedback gain, and noise figure. Additional models include an LTV model[16] and an NLTV configuration using a perturbation model based on numerical techniques.[17-20]

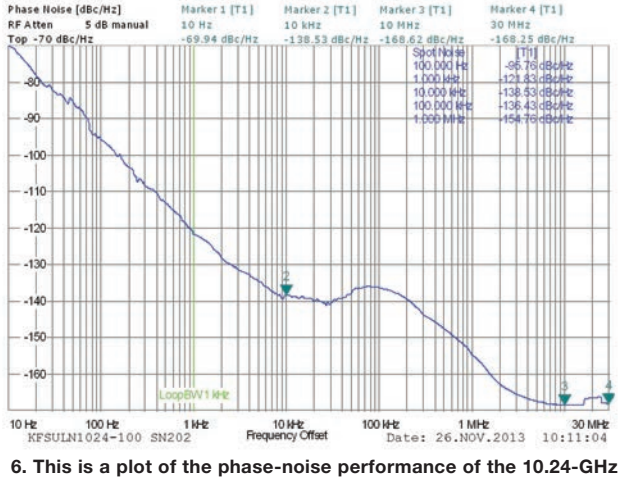
Phase noise has been analyzed by means of a number of different models, with both time- and frequency-domain techniques applied.[21-26] (The relative strengths and weaknesses of the three phase-noise models are compared in *Table 2*, included in the online version of this article). When comparing noise models for harmonic (LC-resonator-type) and nonharmonic oscillator circuits (RC-oscillator-type) oscillator circuits, a designer must choose the noise model, since none of the models provide closed-form solutions for phase noise.

In typical implementations, a synthesizer would use a feedback divider to control the frequency produced by the oscillator. The feedback divider's output noise exhibits the same lowpass transfer characteristics [B(s)] as the input noise, with the divider's close-in noise of greater importance than its noise level. Such a divider is built with logic gates, using typical technologies as TTL, CMOS/BiCMOS, and ECL, but rarely as a regenerative divider based on frequency mixers. TTL dividers can achieve low noise levels[28], to –170 dBc/Hz, with good close-in noise, but their maximum clock frequency rarely exceeds 150 MHz.

Reducing the reference frequency from 100 MHz to 10 MHz would result in degradation of output phase noise of 20 dB, making the TTL divider unsuitable for locking with 100-MHz signals. CMOS/BiCMOS dividers can achieve similar noise levels at offsets greater than 10 MHz, but with more flicker in higher close-in noise levels that makes them poor choices for low-noise synthesizers. A better choice would be using ECL dividers, which typically exhibit noise levels of –155 dBc/Hz.



5 This measurement setup was used to test the DRO reference synthesizer.



6. This is a plot of the phase-noise performance of the 10.24-GHz signal produced by the KFSULN1024-100 source.

Direct frequency synthesis can achieve lower noise than when using feedback dividers and phase-detector combinations. Direct synthesis employs harmonic multipliers, based on step-recovery, PIN, or Schottky diodes, to generate higher-frequency signals. Such diodes allow multiplication of the 100-MHz signal from an OCXO with minimal degradation in noise, with an equivalent noise floor of about −174 dBc/Hz. The synthesis approach can achieve a slightly better noise performance when using references having power levels considerably higher than 0 dBm. The drawback of this method is the high far-offset output noise, with 20logN degradation.

LOWERING NOISE

Improved noise performance can be achieved by combining the direct frequency synthesis approach with a PLL method. A high-frequency phase detector is used to lock the oscillator to the harmonic of the reference clock produced by diode harmonic multipliers. By using a low-noise OCXO with a low-noise high-frequency oscillator, such as a DRO or SAW oscillator, this hybrid method is capable of achieving excellent noise levels. Close-in performance is determined by the OCXO and harmonic multiplier, while far-offset performance is determined by the high-frequency oscillator.

The KFSULN1024-100 DRO reference synthesizer is an implementation of such an approach, providing a 10.24-GHz output signal with low noise. The design locks a 10.24-GHz DRO from Synergy Microwave Corp. (www.synergymwave.com) to the harmonics of an internal OCXO reference, using a low-noise PLL with double-balanced mixer serving as phase detector. By using frequency multiplication from the reference, the noise performance required from the mixer and loop filter is relaxed by about 40 dB. The design employs low-noise operational amplifiers to achieve low noise levels.

The synthesizer was characterized with a model FSUP signal source analyzer from Rohde & Schwarz (www.rohde-schwarz.com). The synthesizer and test system were both placed inside a Faraday cage to minimize the effects of outside noise sources. *Figure 5* shows the test system, while *Fig. 6* shows the test results. The synthesizer produces a +10-dBm signal at 10.24 GHz. The low-noise internal OCXO determines the synthesizer's performance for offset frequencies between 10 Hz and 1 kHz, with −70-dBc/Hz phase noise at 10-Hz offset and −121 dBc/Hz at 1-kHz offset. Low-noise

synthesis techniques produce a low noise floor of –138 dBc at 10-kHz offset. Above 1 MHz, the noise floor is determined by the DRO and reaches –168 dBc/Hz. MW

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