

Low Noise Tuning Diodes for Voltage-Controlled Oscillators

Ulrich L. Rohde

Synergy Microwave, Paterson, N.J., Center for Integrated Sensor Systems, Universität der Bundeswehr, Munich, Germany

Ignatz Eisele

Center for Integrated Sensor Systems, Universität der Bundeswehr, Munich, Germany, Fraunhofer EMFT, Munich, Germany

Leonhard Sturm-Rogon, Robert Wieland and Wilfried Lerch Fraunhofer EMFT, Munich, Germany

An oscillator noise model distinguishes between various noise sources and predicts their influence on voltage-controlled oscillator (VCO) single sideband noise. Tuning diodes are the most critical elements. A test oscillator validates the predicted performance. An equivalent noisy resistor is introduced as a figure of merit for low noise diodes. Finally, the important fabrication considerations for low noise diodes are presented and validated in the test oscillator. At 10 kHz offset, the noise contribution of optimized tuning diodes in the oscillator adds only 10 dB of noise compared to a fixed capacitor design.

For the main single sideband noise contribution the main single sideband noise contribution comes from the transistor's intrinsic noise sources and the noise contribution of the tuning diode. The published flicker noise exponent (AF) and flicker noise coefficient (KF) values for transistors are usually determined at μ V RF levels and normal DC operating conditions. As the RF level in an oscillator is much greater, this must be considered in the circuit analysis.

Most semiconductor companies changed their production processes for tuning diodes due to requirements of digital applications with the result that oscillator phase noise deteriorated. Also, none of the diode manufacturers specifies phase noise in oscillators, as there are too many variations of oscillator circuits available.

To develop and characterize low noise tuning diodes, it is necessary to describe the appropriate oscillator, analyze its critical semiconductor components and



 \bigstar Fig. 1 Generalized oscillator circuit using an amplifier model. Z_L is the load.

finally compare the tuning diode with the ideal case of a fixed capacitor. This article follows that guideline to verify the quality of newly developed tuning diodes.

ANALYSIS OF THREE-REACTANCE OSCILLATORS

A generalized circuit for an oscillator is shown in **Figure 1**. This is typically referred to as a Colpitts oscillator.¹ It has a capacitive voltage divider, Z_1 and Z_2 , and an inductor Z_3 . Its phase noise can be determined with a microwave simulator. With these programs, however, it is not possible to distinguish the individual noise contributions to the output signal. Therefore, a direct analysis of the oscillator circuit equations is presented here. The active device is a three-terminal device, typically a transistor.²

Figure 2 shows the Colpitts oscillator including leads and package parasitics. In practice, the lossy part of a tuned circuit is the inductor. R_{s1} is the resonator loss. Splitting the input impedance Z_{IN} (see Figure 1) of the Colpitts oscillator into real and imaginary parts we obtain:

$$R_{NEQ} = \frac{R_{N}}{\left(1 + \omega^{2} Y_{21}^{2} L_{p}^{2}\right)}$$
(1a)
$$\frac{1}{C_{EQ}} = (1b)$$
$$\left\{ \frac{1}{\left(\frac{1}{C_{1} + C_{p}\right)C_{2}}}{\left(\frac{1}{C_{1} + C_{2} + C_{p}}\right)} - \left[\frac{\omega^{2} Y_{21} L_{p}}{\left(1 + \omega^{2} Y_{21}^{2} L_{p}^{2}\right)}\right] \left[\frac{Y_{21}}{\omega(C_{1} + C_{p})C_{2}}\right] \right\}$$
MWJOURNAL.COM = OCTOBER 2022



A Fig. 2 Colpitts oscillator with base lead inductances, L_p , and package capacitance C_p .^{3, p. 132}

Where:

 R_{N} : Negative resistance without lead inductance and package capacitance

R_{NEQ}: Negative resistance with base-lead inductance and package capacitance

 C_{EQ} : Equivalent capacitance with base-lead inductance and package capacitance.

The method shown is based on one-port oscillator design.^{3,4,5} The negative real part of Z_{IN} compensates the resistor loss of the parallel tuned circuit.

Equation (1b) can be solved for C_{EQ} , see equation (2a), imaginary part. The exact calculation of the "noisy" negative real part of the resistance $Z_{IN', package}$, which is needed to compensate the tuned circuit loss, is given by:

$$Z_{in}|_{package} =$$
 (2a)

$$-\left[\frac{Y_{21}}{\omega^{2}(C_{1}+C_{p})C_{2}}\frac{1}{(1+\omega^{2}Y_{21}^{2}L_{p}^{2})}\right] - j\left[\frac{(C_{1}+C_{p}+C_{2})}{\omega(C_{1}+C_{p})C_{2}}-\frac{\omega Y_{21}L_{p}}{(1+\omega^{2}Y_{21}^{2}L_{p}^{2})}\frac{Y_{21}}{\omega(C_{1}+C_{p})C_{2}}\right]$$

The left part is the negative part of the "noisy" input resistance. The intrinsic value R_{N} is:

$$R_{\rm N} = -\frac{Y_{21}}{\omega^2 C_1 C_2}$$
(2b)

This is a noisy electronically generated negative resistance. It combines all internal noise sources to be modulated on the oscillator carrier frequency.

Leeson's Empirical Phase Noise Model

E.J. Baghdady et al.⁶ first gave the definition of phase noise. Single sideband phase noise equation (3) is based on David Leeson,⁷ Scherer and Rohde.⁸ Scherer was the first to introduce the flicker effect to the Leeson equation and Rohde the first to add the AM-to-PM (VCO, last term in the equation) conversion effect, caused by the nonlinear capacitance of the active devices.

Lesson's complete phase noise equation is given by:

$$\left\{ \left[1 + \frac{f_0^2}{(2f_m Q_L)^2} \right] \left(1 + \frac{f_c}{f_m} \right) \frac{FkT}{2P_{sav}} + \frac{2kTRK_0^2}{f_m^2} \right\}$$
(3)

Where:

 $\pounds(f_m)$ = ratio of sideband power in 1 Hz bandwidth at f_m to total power in dB

f_m = frequency offset, or modulating frequency

 $f_0 = center frequency$

 $f_c = flicker corner frequency$

 Q_L = loaded Q of the tuned circuit, should be half of the unloaded resonator Q_0 (Matching for Power)

F = large signal noise factor

 $kT = 4.1 \times 10^{-21}$ at 300 [K] (room temperature)

 P_{sav} = average power at oscillator output

R = equivalent noise resistance of tuning diode (typically 200 [Ω] to 10 [k Ω])

 $K_0 = oscillator voltage gain$

k = Boltzmann constant.

Equation (3) is shown graphically in **Figure 3**. The problem is that necessary data, like output power, large signal noise figure, loaded Q and flicker noise are not known a priori. The other problem is that it does not provide the actual noise contribution of the semiconductor devices. It is shown below that the phase noise contribution of the tuning diode in VCOs is the critical part, and not the transistor itself. The fixed frequency oscillator is the best phase noise case.

Depending on the relation between f_c and $f_0/2Q_L$, there are two cases of interest. For the low-Q case the spectral phase noise is unaffected by the Q of the resonator, but the L(f_m) spectral density will show a 1/ f^3 and 1/ f^2 dependence close to the carrier. For the high Q case, a region of 1/ f^3 and 1/f should be observed near the carrier.

At small offset frequencies from the carrier, the phase noise exhibits a slope of $1/\Delta f^3$, i.e. 30 dB per decade. This



▲ Fig. 3 Equivalent feedback models of oscillator phase noise.^{3,8}

TABLE 1 f _c vs. I _C	
I _C (mA)	f _c (kHz)
0.25	1
0.5	2.74
1	4.3
2	6.27
5	9.3

(Source: Motorola)

region is dominated by flicker noise up-conversion. Particularly, in CMOS this is a challenge, since the 1/fnoise corner frequency is very high. Above that, the slope is 20 dB per decade. This is the offset frequency region dominated by thermal noise up-conversion. Finally, at higher offset frequencies from the carrier the spectrum is flat, limited by the noise floor of the active circuit (see Figure 2), given by kTF/P_{sig}.⁹ For very high Q resonators, the flicker corner frequency f_c moves to higher frequencies, independent of the transistor (filter effect).

Table 1 shows f_c as a function of the collector current I_C for a typical small-signal microwave bipolar junction transistor (BJT). $I_{C(max)}$ of this transistor is about 10 mA. The corner frequency increases non-linearly with current (DC).

Note that f_c , which is defined by AF and KF in the SPICE model, increases significantly with I_c . This gives a clue about how f_c changes when a transistor oscillates at differ-



Fig. 4 Colpitts oscillator circuit configuration.

ent current levels. Because of the bias-point shift that occurs during oscillation, an oscillating BJT's average I_C is higher than its small-signal I_C . KF is therefore higher for a given BJT operating as an oscillator than for the same transistor operating as a small-signal amplifier. Generally, f_c varies with device type as follows: Si JFETs, 50 Hz and higher; microwave RF BJTs, 1 to 10 kHz (as above); MOSFETs, 10 to 100 kHz and GaAs FETs, 10 to 100 MHz.

Several observations can readily be made. One obvious way to reduce phase noise is to increase the power or oscillation amplitude. This, however, is limited in practical oscillators due to the supply level. Another, more practical, possibility is to increase the quality factor of the tank. The first part of equation (1), describing $1/\Delta\omega^2$, corresponds to the thermal noise part of the spectrum. Multiplying by another $1/\Delta\omega$ describes the flicker noise part of the phase noise spectrum. Flicker noise is described empirically, and no insight is provided into the flicker noise upconversion mechanisms; however, it can still be concluded that increasing the voltage swing or increasing the quality factor of the tank will reduce flicker noise in this region.

Equation (4),⁹ based on Leeson's equivalent circuit and the special case of the Colpitts oscillator, yields exact values for P_{sav} , Q_L and F that are needed to solve Leeson's equation. The approach shown here is novel. We can now calculate the output power. The factor of 1000 is needed since the result is expressed in dBm and a function of n and C_1 .

$$\begin{bmatrix} P_{0}(n, C_{1}]_{dBm} = \\ 10Log \left\{ \begin{bmatrix} \frac{(V_{ce} = -0.7)^{2}}{4(\omega_{0}L)^{2}} \end{bmatrix} \begin{bmatrix} \frac{Q_{L}^{2} \left[C_{1}^{2} \left(\frac{C_{1}}{n-1}\right)^{2} \omega_{0}^{4}L^{2}\right]}{Q_{L}^{2} \left(C_{1} + \frac{C_{1}}{n-1}\right)^{2} + \omega_{0}^{4}L^{2}C_{1}^{2} \left(\frac{C_{1}}{n-1}\right)^{2}} \end{bmatrix} R_{L} * 1000 \end{bmatrix}$$

Where 0.7 V is the high current saturation voltage and V_{ce} is the collector emitter voltage < V_{cc} .

To calculate the loaded Q (Q_L) consider the unloaded Q (Q₀) and the loading effect of the transistor. There we consider the influence of the large signal condition Y_{21}^* . The inverse of this is responsible for the loading and reduction of Q_L.

$$Q^{*} = \frac{\omega_{0} \times \left| \frac{1}{Y_{21}^{*}} \right| (C_{1} + C_{2})}{1 - \omega_{0}^{2} C_{1} L (Q = Q_{0})};$$
(5)

and finally
$$Q_L = \frac{Q_0 x Q^*}{Q_0 x Q^*}$$

The transistor noise factor can also be calculated under large signal conditions. Considering Y_{21}^{*} , this noise calculation is based on general noise calculations

such as those of Pucel and Rohde.¹⁰ An equivalent procedure can be found for FETs as well.

Oscillator Noise Factor

Figure 4 shows the oscillator equivalent circuit configuration for the purpose of analyzing F with respect to the oscillator feedback components (C_1 and C_2),

which are needed to predict F in Leeson's Equation. The objective is to determine the oscillator circuit parameters that influence F, thereby influencing oscillator phase noise.

F for the transistor in Figure 4 is:

$$F = 1 + \frac{Y_{21}^*C_2C_C}{(C_1 + C_2)C_1}$$
(6)
$$\left[\Upsilon_b + \frac{1}{2\Upsilon_e} \left(\Upsilon_b + \frac{(C_1 + C_2)C_1}{Y_{21}^*C_2C_C}\right)^2 \left(\frac{1}{\beta} + \frac{f^2}{f_T^2}\right) + \frac{\Upsilon_e}{2}\right]$$

For fixed capacitors $C_1,\ C_2,\ the following components contribute to oscillator noise:$

- Thermal noise associated with the loss resistance of the resonator
- Thermal noise associated with the base resistance of the transistor
- Shot noise associated with the base bias current



Fig. 5 Oscillator calculation using the ABCD matrix.^{3, p. 132}

• Shot noise associated with the collector bias current. An oscillator circuit with the contribution of all four noise sources is shown in *Figure 5*.

Using an oscillator circuit with a noisy resonator, the total noise of the oscillator in Figure 5 can be determined.³ Consider the effective capacitance C_{eff} :

$$C_{\rm eff} = C + \frac{C_1 C_2}{C_1 + C_2}$$
(7)

The phase noise contribution (PN) from the oscillator circuit with a 2-port [ABCD] matrix is:

$$PN_{in\Upsilon} \left(\omega_{0} + \Delta \omega \right) = \frac{4KT}{Rp} \left[NFT_{in\Upsilon} \left(\omega_{0} \right) \right]^{2} = \frac{4KT}{Rp} \left\{ \frac{1}{2} \left[\frac{1}{2\omega_{0}C_{eff}} \right] \left[\frac{\omega_{0}}{\Delta \omega} \right] \right\}^{2}$$
(8a)

= the phase noise contribution from the resonator tank.

$$PN_{Vbn}(\omega_{0} + \Delta \omega) = 4KT\Upsilon_{b} \left[NFT_{Vbn}(\omega_{0}) \right]^{2} = 4KT\Upsilon_{b} \left\{ \frac{1}{2} \left[\frac{C_{1} + C_{2}}{C_{2}} \right] \left[\frac{1}{2Q} \right] \left[\frac{\omega_{0}}{\Delta \omega} \right] \right\}^{2}$$
(8b)

= the phase noise contribution from the base spreading resistance.

$$PN_{ibn}(\omega_{0} + \Delta\omega) = 2qI_{b}\left[NFT_{ibn}(\omega_{0})\right]^{2} = 2qI_{b}\left\{\frac{1}{2}\left[\frac{C_{2}}{C_{1} + C_{2}}\right]\left[\frac{1}{\omega_{0}QC_{eff}}\right]\left[\frac{\omega_{0}}{\Delta\omega}\right]\right\}^{2}$$
(8c)

= the phase noise contribution from the base current.

$$PN_{ifn}(\omega_{0} + \Delta\omega) = \frac{K_{f}l_{b}^{AF}}{f_{m}} \left[NF_{ibn}(\omega_{0}) \right]^{2} = \frac{K_{f}l_{b}^{AF}}{f_{m}} \left\{ \frac{1}{2} \left[\frac{C_{2}}{C_{1} + C_{2}} \right] \left[\frac{1}{2\omega_{0}QC_{eff}} \right] \left[\frac{\omega_{0}}{\Delta\omega} \right] \right\}^{2}$$
(8d)

= the phase noise contribution from the flicker noise of the transistor.

$$PN_{icn}(\omega_{0} + \Delta\omega) = 2ql_{c} \left[NFT_{icn}(\omega_{0}) \right]^{2} = 2ql_{c} \left\{ \frac{1}{2} \left[\frac{C_{2}}{C_{1} + C_{2}} \right] \left[\frac{1}{2\omega_{0}QC_{eff}} \right] \left[\frac{\omega_{0}}{\Delta\omega} \right] \right\}^{2}$$
(8e)

= the phase noise contribution from the collector current.

AM-to-PM Conversion

The transition from a basic oscillator to a VCO is achieved by replacing all or a part of the resonator capacitor with a voltage dependent variable capacitor, typically a tuning diode or varactor.² The RF voltage across the depletion capacitance modulates the operating frequency. FM and PM cannot be distinguished at a constant f_m ;

however, with a change in f_m , the FM modulation index will change and the PM modulation index will not.

To calculate the total phase noise, an equivalent noise resistance R_{eq} of the tuning diode is defined. When inserted in Nyquist's equation it results in a frequency offset dependent noise voltage $V_{\rm n}$ across the tuning diode:

$$V_{n} = \sqrt{4kTR_{eq}\Delta f}$$
(9)

where kT = 4.2 \times 10×-^21 at 300 K, and Δf is the offset from the carrier.

This noise voltage generated from the tuning diode is now multiplied with the VCO gain K_o, resulting in an rms frequency deviation Δf_{rms} . This can be translated into an equivalent peak phase deviation θ_d :

$$\theta_{\rm d} = \frac{K_{\rm o}\sqrt{2}}{\Delta f} \times V_{\rm n} \text{ rad in a 1 Hz bandwidth}$$
(10)

This is converted into the single sideband (SSB) signal-to-noise ratio expressed in dB

$$SSB S/N = 20 \times \log(\theta_d / 2) dB$$
(11)

Comparing the SSB noise of the oscillator with a fixed capacitor and an identical capacitance value of the tuning diode determines the equivalent noise resistor R_{eq} . The lower the resistor the better the quality of the diode. All relevant information is provided by Rohde and Rudolph.⁹

DIODE FABRICATION AND SINGLE DEVICE PERFORMANCE

A Si tuning diode consists of a p-n junction. Contacting an n-doped and a p-doped region, the mobile charge carriers (electrons and holes) are pulled away from the junction and a depletion zone is created that acts as a capacitor. By applying a reverse bias voltage (V) the depletion zone width x_D increases. For the ntype region it is given by:

$$X_{\rm D} = \sqrt{\frac{2\varepsilon_0 \varepsilon_{\rm Si}}{e N_{\rm D} (X)}} (V_{\rm D} + V)$$
(12)

 $\epsilon_0 \epsilon_{Si}$ is the dielectric constant of Si, e is the elementary charge and $N_D(x)$ is the donor concentration. The diffusion voltage V_D is given by:

$$V_{\rm D} = \frac{W_{\rm C} - W_{\rm F}}{\rm e} \tag{13}$$

where $\rm W_{c}$ is the energy of the conduction band edge and $\rm W_{F}$ is the Fermi energy.

For the p-type region, the donor concentration is replaced by the acceptor concentration.

The voltage dependent capacity C(V) can be written as:

$$C(V) = \frac{A\varepsilon_0 \varepsilon_{Si}}{X_D} = C_0 / \left(1 + \frac{V}{\phi}\right) \gamma$$
(14)

where $\gamma = 0.5$ characterizes the theoretical value for an abrupt junction diode with constant doping concentration in the depletion zone.

For a VCO, several more parameters must be considered, such as frequency range, linearity, series resistance and noise level. So-called hyperabrupt tuning diodes¹¹ are widely used for VCOs and this article presents results regarding these requirements. Using epitaxy, ion implantation and careful thermal management, high-quality hyperabrupt diodes are realized with extremely low noise levels.

Highly doped n-type 200 mm Si wafers with (100) orientation are used to achieve low series resistance. In a first step, an n-type epitaxial layer with a thickness of several micrometers and a doping concentration in the



▲ Fig. 6 SIMS profile of the hyperabrupt tuning diode.

range of 1×10^{15} to 1×10^{16} cm $^{-3}$ is grown. The p+-region is fabricated by ion implantation.

A SIMS profile of the total stack after annealing is shown in **Figure 6**. In principle it is possible to create even sharper doping transitions,¹² however, these techniques (e.g. molecular beam epitaxy) are not suited for mass production. To avoid lateral spreading of the electric field, a guard ring structure is integrated. Diodes with an active area of A = 0.118 mm² as well as A = 0.037 mm² are fabricated on the same wafer.



▲ Fig. 7 Diode equivalent circuit.

For the front-side metallization a Ti/ TiN barrier is sputtered followed by Al/1%Si. For the backside a goldbased metallization is chosen to enable soldering in the package.

The noise of the hyperabrupt diodes—and therefore the resonator noise—depends on the quality factor Im(Z)/Re(Z). The higher the quality factor of the resonator, the lower the oscillator noise. Considering the equivalent circuit of the diode (see **Figure 7**), one must consider two parameters:

1) The crystalline quality of the Si in the depletion zone should be as high as possible to avoid any point defects such as vacancies or interstitials, which act as scattering centers and increase the noise level.¹³ As a consequence, the resistance R_r for



A Fig. 8 Capacitance tuning range vs. reverse bias on the A = 0.118 mm^2 diode measured at 500 MHz.

reverse bias must be as high as possible. This can be achieved by careful annealing steps.

2) The real part of the impedance, which mainly consists of the contact series resistances and the wiring of the package, must be minimized. For this purpose, the wafers are thinned to 120 μ m. The resulting series resistance R_s of the bare die, measured at 5 GHz and 2 V reverse bias voltage, amounts to 0.8 Ω for the larger diode and 1.3 Ω for the smaller diode.

Wafer Level Measurements

The breakdown voltage for both types of diodes is 31 V. For the larger diodes, wafer level measurements of capacitance (measured at 500 MHz) as a function of reverse bias voltage is shown in *Figure 8*. A capacitance $C_1 = 19 \text{ pF}$ is measured at a reverse bias of 1 V and $C_{25} = 2 \text{ pF}$ at 25 V. The resulting capacitance ratio C_1/C_{25} is 9.5.

For the smaller diodes, capacitance versus voltage behavior is shown in **Figure 9**. A capacitance $C_1 = 6.2 \text{ pF}$ is measured at a reverse bias of 1 V and $C_{25} = 0.75 \text{ pF}$ at 25 V. The resulting capacitance ratio C_1/C_{25} is 8.3.

In contrast to the above derived simple depletion approximation,



A Fig. 9 Capacitance tuning range vs. reverse bias on the A = 0.037 mm^2 diode measured at 500 MHz.



Fig. 10 γ vs. bias voltage for the A = 0.118 mm² diode measured at 500 MHz.



Fig. 11 γ vs. bias voltage for the A = 0.037 mm² diode measured at 500 MHz.



🔺 Fig. 12 1.3 GHz test oscillator with tuning diodes (a) and schematic (b).



▲ Fig. 13 Measured phase noise of the oscillator with a fixed capacitor.

the γ -value of hyperabrupt tuning diodes is no longer constant with reverse bias, however, this value is important for the design of oscillators. Therefore, wafer level measurements are made for the two types of diodes (see *Figures 10* and *11*).

Packaging

After wafer level measurements the wafers are diced and packaged in a QFN type housing with SC79 soldering pads. The front-side contact, which acts as anode, is gold wire bonded, whereas the backside contact, which acts as cathode, is connected to the ground plate. The lead frame is copper.

SIMULATION AND MEASUREMENT OF PHASE NOISE IN A TEST OSCILLATOR

Noise performance of diodes can only be characterized in a test oscillator. It should be noted that different results are obtained for different oscillator designs. The quality of the diodes is demonstrated with the Infineon transistor BFP 620 in an oscillator at 1.3 GHz (see *Figure 12*).

Instead of the tuning diodes, we start with a fixed capacitor of 15.3 pF in parallel with the 0.7 pF capacitor to ground (see Figure 12b), for a frequency of about 1.3 GHz. This is the ideal case and acts as a reference.



▲ Fig. 14 Oscillator phase noise without a tuning diode calculated using Leeson's equation (a) and simulated using the Serenade HB microwave simulator (b).

The measured phase noise of this circuit as a function of frequency offset from the center frequency is shown in *Figure 13*. At an offset of 10 kHz it is about -115 dBc/ Hz. An offset frequency of 10 KHz is used as this is the closest to the carrier selected in a PLL to compensate microphonic effect and outside the PLL loop frequency where the inherent phase noise dominates. The prediction from the presented model as well as the SPICE data-based simulation (see *Figure 14*) agrees well with the measurement.

Next, the capacitor is replaced by a tuning diode to realize a VCO. According to Figure 8, a reverse bias of about 2 V is needed to obtain a comparable capacitance of 15 pF. The resulting measured phase noise plot of the oscillator is shown in *Figure 15*. The phase noise at a 10



▲ Fig. 15 Measured phase noise of the oscillator with tuning diodes.

kHz offset is about -107 dBc/Hz, only 8 dB above the level with a fixed capacitor, for an oscillator with a 2 to 1 tuning range. To our knowledge, this is the best value achieved to date.

Equations 9 and 10 are used to perform a backward calculation for the equivalent noise resistor.

For L(f_m) =-107.41 dBc/Hz, assuming a K₀ of 120 MHz/V, Δf_{rms} = 0.06 in a 1 Hz bandwidth.

$$\theta_{d} = \frac{K_{o}\sqrt{2}}{f_{m}} \times V_{n} =$$

$$\frac{120 \times 10^{6}\sqrt{2}}{f_{m}} \times 5.02 \times 10^{-10} =$$

$$8.519 \times 10^{-6} \text{rad in}$$
1 Hz bandwidth
(15)

For an offset frequency

$$f_{\rm m} = 10 \, \rm kHz \, \theta_{\rm d} = 8.519 \times 10^{-6} \, / \, f_{\rm m}$$

$$\theta_{d} = \frac{K_{o}\sqrt{2}}{f_{m}} \times V_{n} = \frac{8.519 \times 10^{-6}}{10,000} =$$

rad 1Hz bandwidth (16)

$$Log(\theta_{d} / 2) = log(4.26E - 6) = -5.37;$$

L = 20xlog(\theta_{d} / 2) =
-107 dBc / Hz, QED (17)

The resulting voltage value $V_n = 5.02 \times 10^{-10}$ $V_{\sqrt{Hz}}$. Finally, the newly developed diodes have a very low equivalent noise resistance of only 15 Ω .

CONCLUSION

The described noise model for VCOs proves that tuning diodes dominate the sideband noise of oscillators. As a figure of merit for the diodes, an equivalent noise resistor is introduced that describes

the noise spectrum deviation from an ideal case with a fixed capacitor. The newly developed diodes with the same AC characteristics as comdiodes mercial demonstrate phase noise levels only 8 dB above the value for a fixed capacitor when measured with the same test oscillator.

References

- 1. E. H. Colpitts, "Oscillation Generator," U.S. Patent No. 1 624 537, February 1918.
- U. L. Rohde and A. M. Apte, "Everything You Always Wanted to Know About Colpitts Oscillators," *IEEE Microwave Magazine*, Vol. 17, No. 8, August 2016, pp. 59–76.
- U. L. Rohde, A. K. Poddar and G. Böck, The Design of Modern Microwave Oscillators for Wireless Applications, John Wiley & Sons, Hoboken, NJ, 2005.
- K. Kurokawa, "Some Basic Characteristics of Broadband Negative Resistance Oscillator Circuits," *The Bell System Technical Journal*, Vol. 48, No. 6, July-August 1969, pp. 1937– 1955.
- U. Rohde, A. Poddar and A. Apte, "How Low Can They Go, Oscillator Phase Noise Model, Theoretical, Experimental Validation, and Phase Noise Measurements," *IEEE Microwave Magazine*, Vol. 14, No. 6, September/October 2013, pp. 50–72.
- E. J. Baghdady, R. N. Lincoln and B. D. Nelin, "Short-term Frequency Stability: Characterization, Theory, and Measurement," *Proceedings of the IEEE*, Vol. 53, No. 7, July 1965, pp. 704–722.
- D. B. Leeson, "A Simple Model of Feedback Oscillator Noise Spectrum," *Proceedings of the IEEE*, Vol. 54, No. 2 February 1966, pp. 329–330.
- G. Vendelin, A. M. Pavio, U. L. Rohde and M. Rudolph, *Microwave Circuit Design Using Linear and Nonlinear Techniques*, John Wiley & Sons, Hoboken, NJ, 2021.
- U. L. Rohde and M. Rudolph, *RF / Microwave Circuit Design for Wireless Applications*, Second Edition, John Wiley & Sons, Hoboken, NJ, 2013.
- R. A. Pucel and U. L. Rohde, "An Exact Expression for the Noise Resistance R/sub n/ for the Hawkins Bipolar Noise Model," *IEEE Microwave and Guided Wave Letters*, Vol. 3, No. 2, February 1993, pp. 35–37.
 R. Kumar and A. Bhattacharyya, "Variability
- R. Kumar and A. Bhattacharyya, "Variability Study and Design Considerations of P-N Junction Hyperabrupt Varactor Diodes," *IEEE Transactions on Electron Devices*, Vol. 24, No. 10, October 1977, pp. 1270–1272.
- I. Eisele, "Delta-Doping Profiles in Silicon," Applied Surface Science, Vol. 36, No. 1–4, 1989, pp. 39–51.
- J. Störmer, P. Willutzki, D.T. Britton, G. Kögel, W. Triftshäuser, W. Kiunke, F. Wittmann and I. Eisele, "A Slow Positron Lifetime Study of the Annealing Behavior of an Amorphous Silicon Layer Grown by MBE," *Applied Physics*, Vol. 61, July 1995.