RECENT ADVANCES IN LINEAR VCO CALCULATIONS, VCO DESIGN AND SPURIOUS ANALYSES OF FRACTIONAL-N SYNTHESIZERS

By
Ulrich L. Rohde*
Günther Klage**

INTRODUCTION

Modern advanced synthesizers take advantage of the fractional synthesis principle where the noise of the synthesizer inside the loop bandwidth is mainly controlled by all the active components and the up multiplication of the reference frequency noise contribution. The main villians here are going to be the phase detector, the reference standard, the reference dividers, and the operation amplifier. The loop bandwidth depends on the reference frequency. A good combination is a reference frequency of more than 10MHz and loop filter bandwidth of 15KHz. This bandwidth cleans up the VCO, specifically avoids microphonic events. In these types of synthesizers it is not uncommon to use a dual time constant filter in which the wider bandwidth helps with acquisition of frequency while the lower bandwidth become effective as phase acquisition will be done. The loop bandwidth of the filter cannot be made infinitely wide and needs to be set at the crossover point, where the phase noise of the active components, as well as the reference, is equal to the VCO noise by itself and if a $\Sigma\Delta$ converter based fractional-N synthesizer is used, its noise corner frequency also becomes relevant.

This paper deals with an improved linear analysis for phase noise in which, for the first time, both loaded and unloaded Q of the VCO circuit is considered, and we will show there is an optimum ratio between the two numbers. Any deviation from either side will show a phase noise deterioration. In addition, we will show the influence of the noise on the fractional synthesizer and its limitations. The limitations are mainly set by the technology of the dividers, phase detectors, and the available minimum division ratios of the principle of the fractional divider itself.

THE VCO

In the frequency range from 400MHz to 4GHz, the main resonators of choice are ceramic resonators and high-Q printed microstrip/stripline resonators. For conventional size oscillators requiring the best phase noise, the CRO approach is preferred. In most cases, a Colpitts oscillator is successfully used. Circuits with grounded base exhibit severe stability problems and even the Colpitts oscillator, based on its emitter circuitry, shows ocassional unwanted resonances up to 6GHz. This is due to the fact that the modern Si and SiGe transistors have so much gain that they become easily unstable and find reactances to satisfy the oscillation requirements (Barkhausen criterion). Once oscillation at the proper frequency has been established, the

* Ulrich L. Rohde, Synergy Microwave Corporation, Paterson, NJ USA, email: ulr@synergymwave.com
** Günther Klage, Rohde & Schwarz, Munich, Germany, email: guenther.klage@rsd.rohde-schwarz.com

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immediate question is how much phase noise will it have. This of course is determined by the large signal flicker corner frequency of the oscillator device, typical values for transistors are AF = 2, KF = 1E-5 to 1E-9. These are the equivalent SPICE parameter values which determine the corner frequency. Microwave transistors typically have a corner frequency between 1 and 5KHz with a tendency that the corner frequency moves up as we move up to higher f_T devices. The flicker corner frequency is defined as the frequency at which the first break point on the phase noise plot occurs if a low Q resonator is used. Figure 1 shows the high and low Q case.

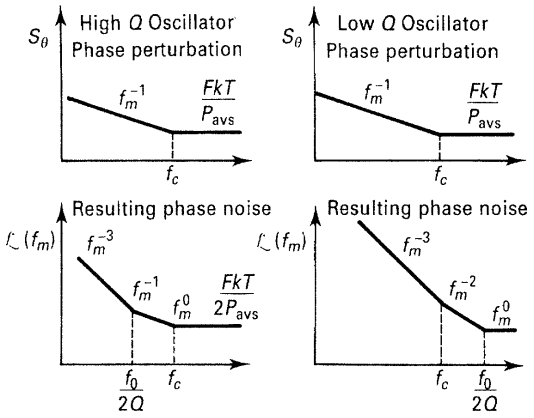

Figure 1 – Oscillator Phase Noise for high-Q and low-Q resonator viewed as spectral phase noise and as noise-to-carrier ratio versus frequency from the carrier.

While the authors still believe that the most accurate way of determining the actual phase noise is the use of a nonlinear simulator with good active device modeling, it is legitimate to use a first order linear approach. There is no linear equation for the bias dependent flicker corner frequency unless AF and KF are used in a nonlinear simulator, but the linear expression allows the use of the "expected" flicker corner frequency in the linear equation legitimately. The third component is the tuning diode, operated in a reverse bias condition. The tuning diode also has AF and KF values, AF being about 2 and KF being about 1E-15. In linear terms we can assign the diode an equivalent noise resistance which, dependent on the technology, varies between 200 and 20K Ω. We are now ready to look at a linear noise calculation.

Leeson (in 1966) introduced a linear approach for the calculation of oscillator phase noise. His formula [1] was extended by Scherer of Hewlett-Packard (HP Application Note), adding the flicker corner frequency calculation to it and Rohde added the VCO term [2]. The phase noise of a VCO is now determined by

$$\mathcal{L}(f_m) = 10\log\left\{\left[1+\frac{{f_0}^2}{(2f_mQ_{load})^2}\right]\left(1+\frac{f_c}{f_m}\right)\frac{FkT}{2P_{sav}(1-\frac{Q_{load}}{Q_0})}+\frac{2kTRK_0{}^2}{{f_m}^2}\right\}$$

where

$\mathcal{L}(f_m)$ = ratio of sideband power in a 1-Hz bandwidth at f_m to total power in dB (spectral density)

f_m = frequency offset
f_0 = center frequency
f_c = flicker frequency
Q_{load} = loaded Q of the tuned circuit
Q_0 = unloaded Q of the tuned circuit; $Q_0 > Q_{load}$
F = noise factor
$kT = 4.1 \times 10^{-21}$ at 300 K (room temperature)
P_{sav} = average power at oscillator output
R = equivalent noise resistance of tuning diode (typically 200 Ω to 10 kΩ)
K_0 = oscillator voltage gain

When adding an isolating amplifier, the noise of an *LC* oscillator is determined by

$$S_\phi(f_m) = \left[a_R F_0^4 + a_E (F_0/(2Q_L))^2\right] / f_m^3$$
$$+ \left[\left(2GFkT/P_0\right)\left(F_0/\left(2Q_L\right)\right)^2\right] / f_m^2$$
$$+ \left(2a_R Q_L F_0^3\right) / f_m^2$$
$$+ a_E / f_m + 2GFkT / P_0$$

where

G = compressed power gain of the loop amplifier
F = noise factor of the loop amplifier
k = Boltzmann's constant
T = temperature in kelvins
P_0 = carrier power level (in watts) at the output of the loop amplifier
F_0 = carrier frequency in Hz
f_m = carrier offset frequency in Hz
$Q_L (= pF_0 t_g)$ = loaded Q of the resonator in the feedback loop
a_R and a_E = flicker noise constants for the resonator and loop amplifier, respectively

More detailed information about this is given in the original paper by Leeson and in [3].

The following table shows the flicker corner frequency f_C as a function of I_C for a typical small signal microwave BJT.

I_C (mA)	f_C (kHz)
0.25	1
0.5	2.74
1	4.3
2	6.27
5	9.3
Source: Motorola	

Figure 3 shows a typical CRO (ceramic resonator-based oscillator). Using the result of a nonlinear simulator, we can compare the measured phase noise and the predicted phase noise. This is shown in Figures 4 and 5. From the phase noise we can determine both the loaded Q and, within limits, the corner flicker frequency. We already stated that for high Q resonator the

flicker corner frequency will shift. For a value Q_{load} of 200 at the center frequency of 800MHz and an f_C = 1000Hz we obtain the same results as measured from the linear equation. Figure 6 shows this. If the diode gets disconnected, the phase noise improves, which means <u>all</u> the noise comes from the tuning diode. Q_0 was set at 400. As Q_{load} approaches Q_0 there is a degradation of the phase noise starting at Q_{load} = 300, getting worse as it approaches 400, where it will be infinite. This is due to the newly introduced term:

$$\left(1-\frac{Q_{load}}{Q_0}\right)$$

Given the conditions: P_{out} = 0dBm, F_0 = 880MHz, R_n = 200Ω, Q_u = 600 at 100KHz off the carrier, we obtain the following values:

Q_{load}	50	100	200	300	400	500	550	580
ℒ(dBc/Hz)	-127	-133	-139	-140	-141	-142	-141	-134

The noise remains fairly flat between a Q of 200 and 550. This is due to the losses of the resonator and the variation of the output level, which is driven by these losses. An unloaded Q of 600 is not easy to obtain. The following plot, Figure 2, shows the phase noise of an oscillator (not VCO) with an unloaded Q of 400. This value is more realistic.

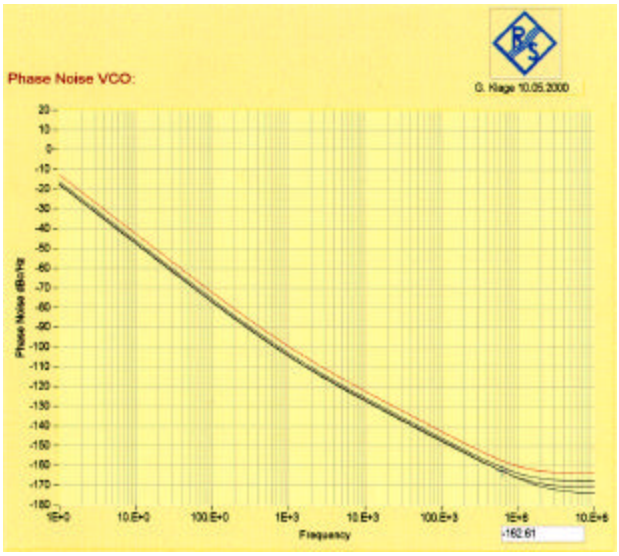

Figure 2 – Phase noise as a function of Q_{load}/Q_0. The lowest curve refers to a Q of 200, the next trace is 300, 350, and finally 380. This shows clearly that if loaded Q gets too high, the oscillator performance deteriorates.

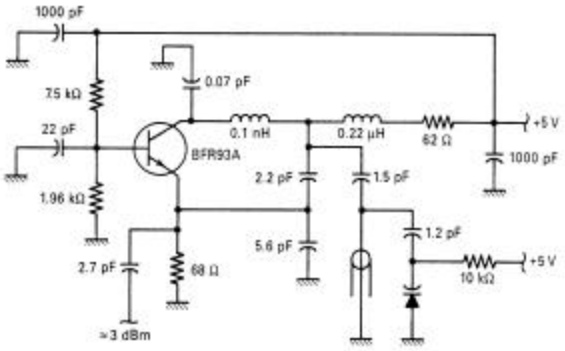

Figure 3 - Schematic of a high-performance ceramic-resonator-based oscillator that can be used from 500MHz to 2GHz, in our case 804.6MHz. The voltage coupling resistor to the diode of 10k Ω in the drawings needs to be replaced with a wideband RF choke.

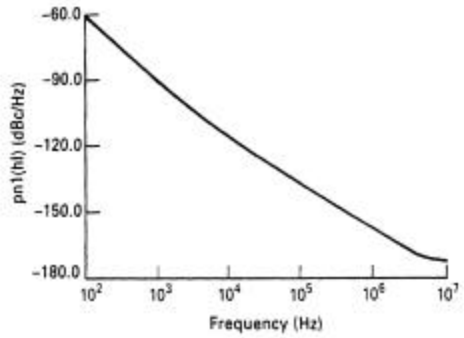

Figure 4 - Simulated phase noise of the oscillator shown in Figure 2.

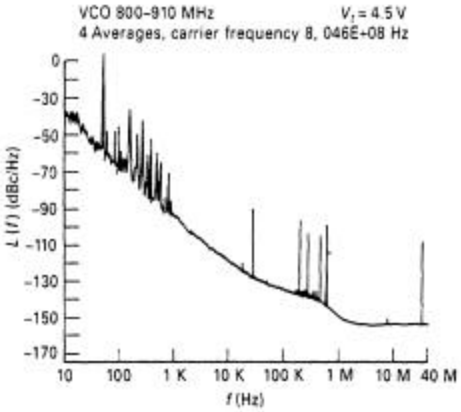

Figure 5 - Measured phase noise of the Oscillator shown in Figure 2. The pedestal above 100KHz comes from the reference oscillator, the model HP-8662.

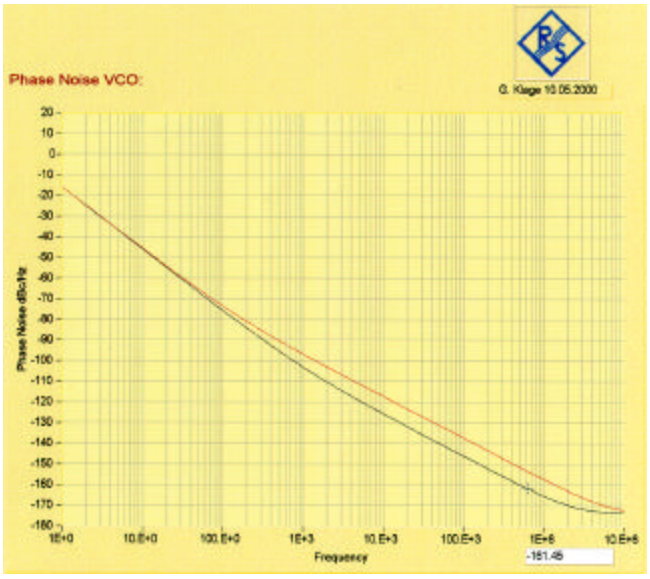

Figure 6 – Phase noise predicted by the linear equation. The top curve shows the oscillator with the tuning diode. The lower curve shows the phase noise of the oscillator itself. The tuning diode dominates.

As mentioned, the influence of the tuning diode, which is shown in the last term of the phase noise equation, dominates the phase noise if the tuning sensitivity gets too high. To get more insight into this Figure 7 shows the noise contribution of the tuning diode(s) as a function of the resulting tuning sensitivity.

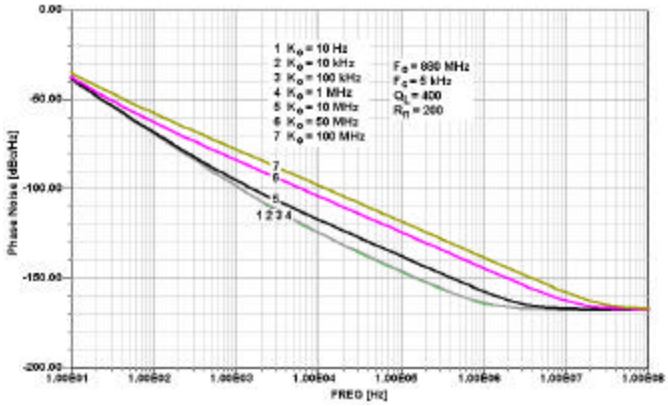

Figure 7 - Predicted phase noise of an 880-MHz VCO with tuning sensitivity ranging from 10 Hz to 100 MHz/V. It *must* be noted that above a certain sensitivity--in this case, 10 MHz/V--the phase noise is determined only by the circuit's tuning diode(s) and is no longer a function of the resonator and diode *Q*.

Additional Modeling Problems

Many authors also assume that all the components are ideal. In reality, passive devices such as capacitors and inductors have "lead inductors" and the connecting points or solder joints also have resistive elements. Therefore, a capacitor is correctly modeled as a series connection of the capacitor itself in series with a small inductor in the vicinity of .2 – 1 nH and a contact resistor of about .2 - .3 Ω. The following circuit diagram shows to what level of detail the modeling must be done so measured and predicted phase noise agree. The particular oscillator is not an award winning design, but both measurements of modeling agree very closely [4].

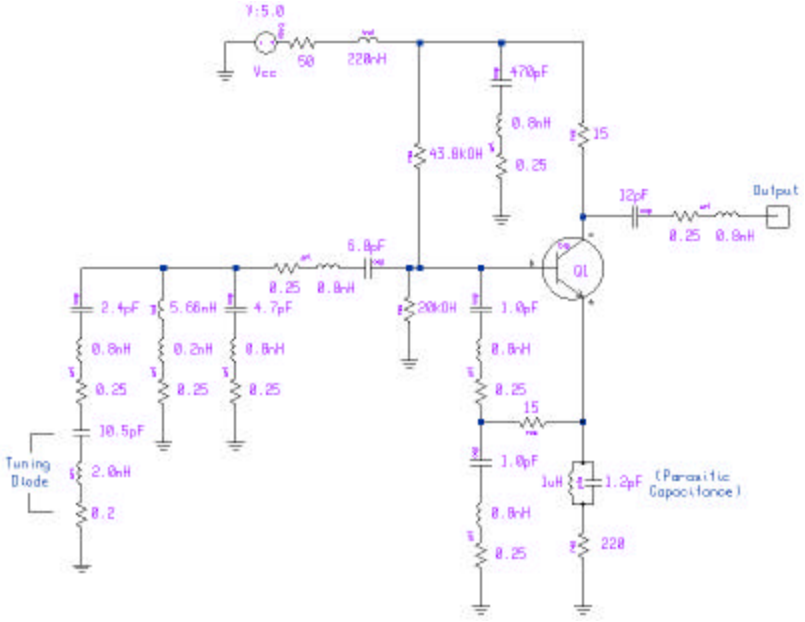

Figure 8 - Colpitts oscillator that uses RF negative feedback between the emitter and capacitive voltage divider. To be realistic, we have also used real components rather than ideal ones. The suppliers for the capacitors and inductors provide some typical values for the parasitics. The major changes are 0.8 nH and 0.25 Ω in series with the capacitors. The same thing applies for the main inductance, which has a parasitic connection inductance of 0.2 nH in series with a 0.25-Ω resistance. These types of parasitics are valid for a fairly large range of components assembled in surface-mount applications. Most engineers model the circuit only by assuming lossy devices, not adding these important parasitics. One of the side-effects we have noticed is that the output power is more realistic and, needless to say, the simulated phase noise agrees quite well with measured data. This circuit can also serve as an example for modeling amplifiers and mixers using surface-mount components.

As a result, the measured and predicted phase noise is extremely close.

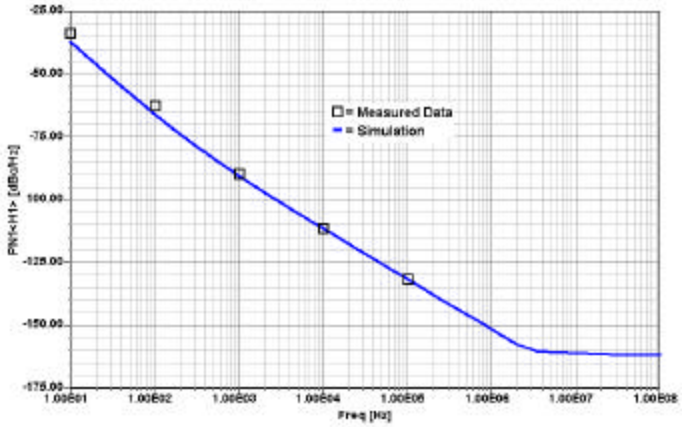

Figure 9 - Comparison between predicted and measured phase noise for the oscillator shown in Figure 8.

IMPROVEMENT OF THE NOISE PERFORMANCE

The linear model is somewhat optimistic since the equation "assumes" a lot of events to be linear and easy to model. In reality, the noise as super-imposed on the ideal noiseless carrier, comes from many contributors. This is best seen in Figure 10 which shows a block diagram of noise sources.

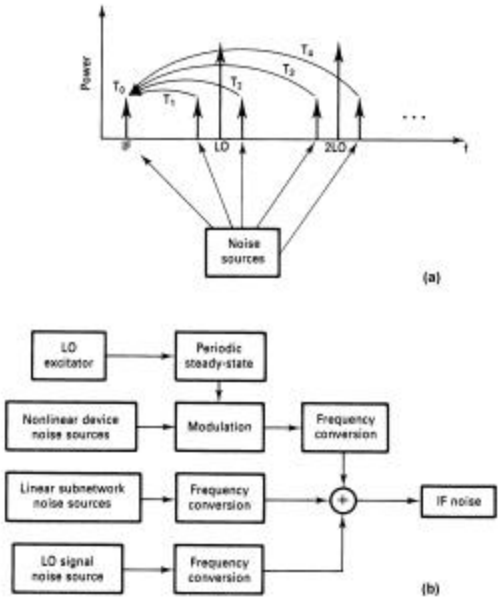

Figure 10 - Summary of (*a*) noise sources mixed to the IF, and (*b*) IF noise contributions.

The noise can be improved by having a resonator circuit with the highest possible Q, provided the tuning diode is not the main villain. When using a transmission line-based resonator instead of a coil inductor, the Thompson formula $F = 1/(2\pi LC)^{.5}$ is no longer valid and the inductance L has to be replaced with a hyperbolic TAN function, $X_L = Z_0 \tanh\left(\frac{2p\ell}{l}\right)$, with $\ell < l/4$. As a result, the circuit has a sharper resonance or appears to have a higher Q. Figure 11 shows the impact on the noise as well as the performance that can be achieved by varying the DC source.

The tuning diode, which because of the PM conversion, adds strongly to the noise, also influences the Q. The standard circuit is to use two diodes instead of one in a anti-series connection which is chosen to avoid DC rectification in self-biasing at RF voltages higher than DC voltages. Figure 12 shows such an arrangement.

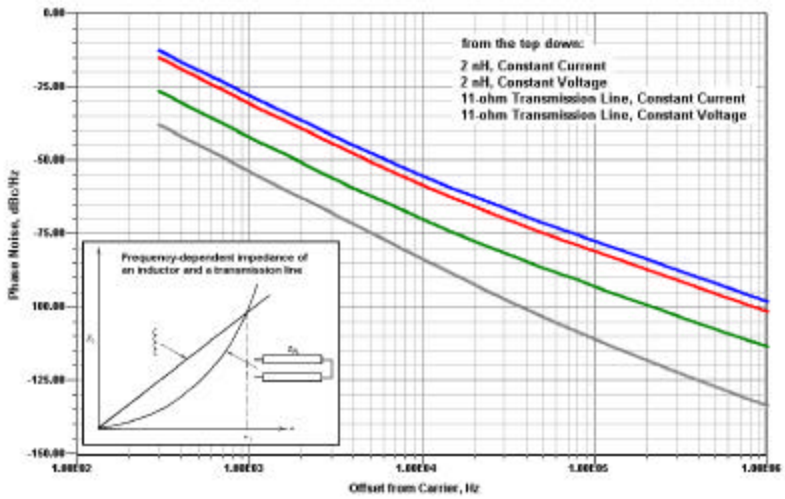

Figure 11 - Transistor oscillators are sensitive to the bias network and to the resonator circuit. As a test we have differentiated constant-current and constant-voltage biasing, as well as interchanging inductors with transmission lines. The phase noise improves with the use of a transmission line and a constant-voltage bias source. (A constant-voltage source prevents a dc bias shift. The dual of a constant voltage at the base is a constant-current source at the emitter.)

Many circuits with medium tuning range rely on one single diode for tuning as we saw in Figure 2. If the tuning range increases the RF voltage swing across the tuning diode increases. A remedy to this is the use of two diodes connected in series where the opposite polarity of the diode cancels the DC rectification. This circuit has the drawback that there are loss resistors in series, therefore, the circuit of choice uses at least two diodes in each series arm. Many applications resort to even a larger number of diode combinations. Much more than four diodes on each side are typically not useful as the total capacitance value makes it fairly high. In the example, Figure 12, the inductor of the left circuit is replace with a shorter stub element, which can be used to model a ceramic resonator.

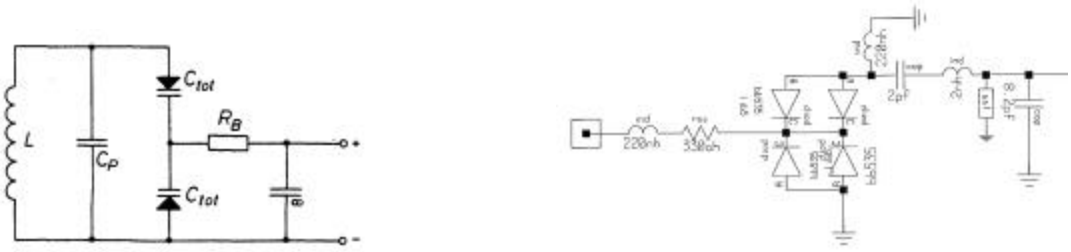

Figure 12 - Parallel-resonant circuit with two tuning diodes, on the left. To reduce the losses the better circuit uses two diodes in parallel on each leg. The shorted stub (SST) is a model element for a ceramic resonator.

Further improvement in the noise can be achieved by DC/RF feedback. The following two circuits sample the DC current as well as the low frequency components in either the emitter or the collector current. By using feedback circuits, one can combine both a DC stabilization as well as a noise compensation/cancellation.

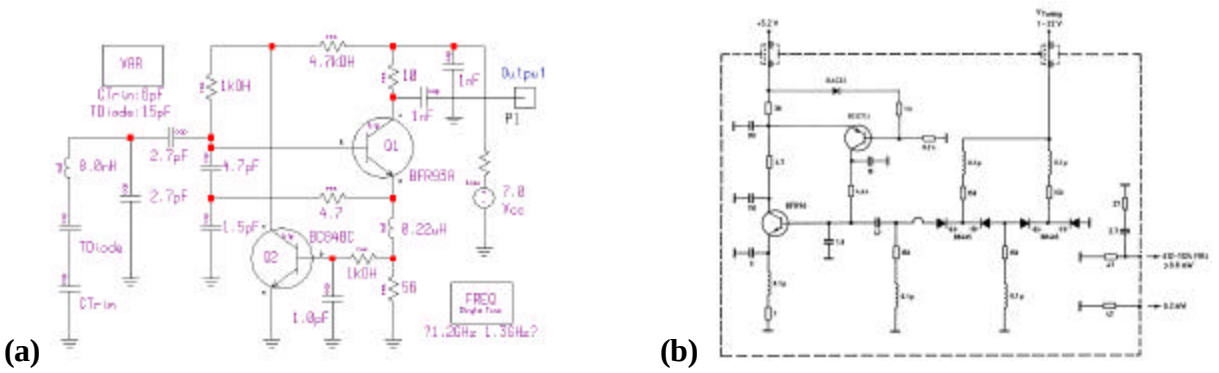

Figure 13 - BJT-based oscillators with noise feedback. At (a), the noise sampling is done in the transistor emitter; at (b), the noise sampling is done in the collector. The biasing with PNP transistor has always been used for grounded emitter microwave circuits, but the feedback loop was so narrow that no noise or feedback/cancellation was possible.

This type of feedback circuit can provide a drastic noise improvement within the loop bandwidth of the circuit used. Figure 14 shows the measured phase noise improvement for such a feedback circuit using a novel design where the oscillator and the feedback are combined in a custom RFIC. For these arrangements there are either already existing patents or patents pending.

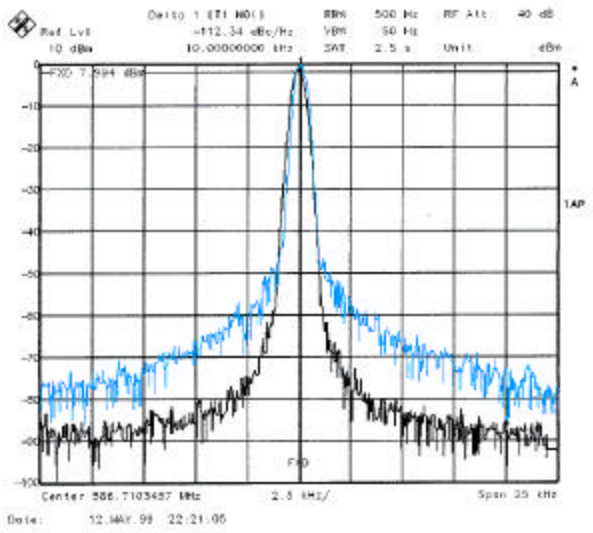

Figure 14 - shows the phase noise improvement caused by a novel RFIC oscillator circuit, which includes a tuning diode. However, the tuning diode coupling is only about 10MHz per volt, and therefore, does not add much to the modulation noise. For test purposes, this is an LC circuit with a loaded Q of 50 measured at about 500MHz. The IC operates up to 3GHz.

This feedback shows an improvement of about 15dB of the phase noise. The noise improvement can be expanded to 1MHz off the carrier if the feedback circuit has the appropriate gain and exactly 180° phase shift within the required bandwidth.

FRACTIONAL-N SYNTHESIZER

The principle of the fractional-N division synthesizer has been around for a while. In the past, implementation of this has been done in an analog system. A single loop synthesizer uses a frequency divider where the division ratio is an integer value between 1 and some very large number, hopefully not as high as 50,000. It would be ideal to be able to build a synthesizer with a reference as high as 50MHz and yet obtain the desired step size resolution such as 25KHz. This would lead to the much smaller division ratio, and therefore, would have a much better phase noise performance.

General purpose designs for synthesizers not only use single loop approaches, but also allow the introduction of an auxiliary frequency which can consist out of a single loop synthesizer or a harmonic sampler. Figure 15 shows a block diagram for a "universal" synthesizer module. It consists of a reference oscillator, which is shown on the top left and is marked reference source. Typically, a high performance crystal oscillator is used here. Reference frequencies from very low values like 10KHz or so up to high frequencies like 100MHz are possible. In this case, a data file was chosen which represents a 10MHz frequency standard. This 10MHz frequency is then divided by 1 (no divider) and connected to the input of the phase detector. For conventional synthesizers, the division ratio would be chosen so the input to phase detector is equal to the step size. On the top right side, we find a voltage controlled oscillator at 200MHz, which after being divided by 20 provides a 10MHz input to the phase detector. Since the auxiliary loop is in the "off" position, this portion does not have any contribution to the system. The software will accept inputs like the noise floor of the dividers, the phase detector sensitivity, the noise voltage of the active filter, and the loop bandwidth. For this single loop synthesizer, the software calculates the total noise and shows the various noise contributions. For a 50KHz loop bandwidth, the solid line shows the resulting total phase noise. At about 200Hz it shows the improvement due to the loop, which has a slight peak around 50KHz, with a phase noise of about –117dBc/Hz. The free-running oscillator we looked at before has a predicted phase noise of about –130dBc/Hz. This means that the loop bandwidth is too wide as it now shows the up multiplication of the noise sources which results in nonfavorable phase noise. The original VCO was not particularly good and yet the system managed to make it even worse. A more appropriate loop bandwidth would have been somewhere around 5KHz where the free running oscillator has a phase noise of about -110dBc/Hz. The dashed line which peaks around 50KHz shows the noise improvement of the VCO due to the loop and then the Q of the oscillator, outside the bandwidth, dominates. The horizontal dashed line at about –130dBc/Hz represents the phase noise of the mixer (not used) and the main divider contribution. The line underneath is the noise level of the operational amplifier (if used) and the phase detector at the VCO frequency.

The current configuration also only allows a step size of 10MHz.

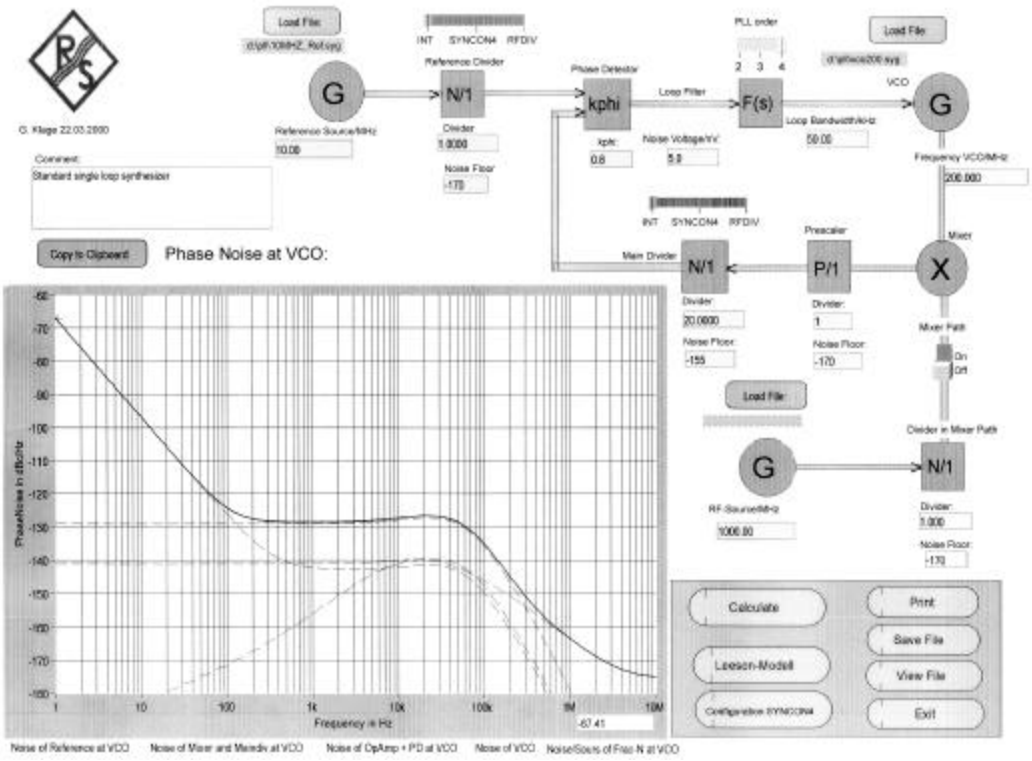

Figure 15 – Picture of the universal synthesizer software screen image with the various contributions as explained in the above text. It can handle single loop synthesizers multi-loop synthesizers, including up multiplication (N < 1) and marked as divider in mixer path. Finally, it also allows to calculate the spurious contents using the fractional synthesizer principle based on the digital compensation scheme. This is done in a separate portion of the software.

An alternative would be for N to take on fractional values. The output frequency could then be changed in fractional increments of the reference frequency. Although a digital divider cannot provide a fractional division ratio, ways can be found to accomplish the same task effectively. The most frequently used method is to divide the output frequency by $N + 1$ every M cycles and to divide by N the rest of the time. The effective division ratio is then $N + 1/M$, and the average output frequency is given by

$$f_o = \left(N + \frac{1}{M} \right) f_r$$

This expression shows that f_o can be varied in fractional increments of the reference frequency by varying M. The technique is equivalent to constructing a fractional divider, but the fractional part of the division is actually implemented using a phase accumulator. The phase accumulator approach is illustrated by the following example.

Example: considering the problem of generating 899.8MHz using a fractional-N loop with a 50 MHz reference frequency, 899.8 MHz = 50 MHz $\left(N + \frac{K}{F} \right)$; the integral part of the division N has to be set to 17 and the fractional part $\frac{K}{F}$ needs to be $\frac{996}{1000}$; (the fractional part $\frac{K}{F}$ is not a

integer) and the VCO output has to be divided by 996 × every 1,000 cycles. This can easily be implemented by adding the number 0.996 to the contents of an accumulator every cycle. Every time the accumulator overflows, the divider divides by 18 rather than by 17. Only the fractional value of the addition is retained in the phase accumulator. If we move to the lower band or try to generate 850.2MHz, N remains 17 and $\frac{K}{F}$ becomes $\frac{4}{1000}$. This simple method of using fractional division was first introduced by using analog compensation to reduce the spurious frequencies, but today it is implemented totally as a digital approach. The necessary resolution is obtained from the dual modulus prescaling, which allows for a well established method for achieving a high-performance frequency synthesizer operating at UHF and higher frequencies. Dual-modulus prescaling avoids the loss of resolution in a system compared to a simple prescaler; it allows a VCO step equal to the value of the reference frequency to be obtained. The dual modulus prescaler then divides by N or N+1 depending upon the state of its control. The only drawback of prescalers is the minimum division ratio of the prescaler for approximately N^2. The dual modulus divider is the key to implementing the fractional-N synthesizer principle. Although the fractional-N technique appears to have a good potential of solving the resolution limitation, it is not free of having its own complications. Typically, an overflow from the phase accumulator, which is the adder with the output feedback to the input after being latched, is used to change the instantaneous division ratio. Each overflow produces a jitter at the output frequency, caused by the fractional division, and is limited to the fractional portion of the desired division ratio.

In our case, we had chosen a step size of 200 kHz, and yet the discrete side bands vary from 200 kHz for $\frac{K}{F} = \frac{4}{1000}$ to 49.8 MHz for $\frac{K}{F} = \frac{996}{1000}$. It will become the task of the loop filter to remove those discrete spurious. While in the past the removal of the discrete spurs has been accomplished by using analog techniques, various digital methods are now available. The microprocessor has to solve the following equation:

$$N^* = \left(N + \frac{K}{F} \right) = \left[N(F - K) + (N + 1)K \right]$$

Example

For $F_O = 850.2MHz$, we obtain:

$$N^* = \frac{850.2MHz}{50MHz} = 17.004$$

Following the formula above:

$$N^* = \left(N + \frac{K}{F} \right) = \frac{\left[17(1000-4) + (17+1) \times 4 \right]}{1000}$$

$$= \frac{\left[16932 + 72 \right]}{1000} = 17.004$$

$$F\ out \quad = 50MHz \times \frac{\left[16932 + 732 \right]}{1000}$$

$$= 846.6MHz + 3.6MHz$$

$$= 850.2MHz$$

The mechanism that generates the digital compensation is seen in Figure 16. This block diagram shows the approach patented by Marconi, European Patent No. 0125790B2, July 5, 1995. It consists of three first order ΣΔ converters which are connected in series and are responsible for a bit manipulation. Only the first accumulator is responsible for the frequency resolution, while the contents of the additional accumulators are responsible for the frequency resolution. This algorithm controls the division ratios. The systems requires a programmable divider in the loop. A simple dual modulus prescaler is not sufficient. More advanced systems incorporate the compensation algorithm digitally in the custom IC. This allows smaller division ratios than 10. The overall patent situation is hairy, but we have not violated any of the patents listed in [3], pages 191-193.

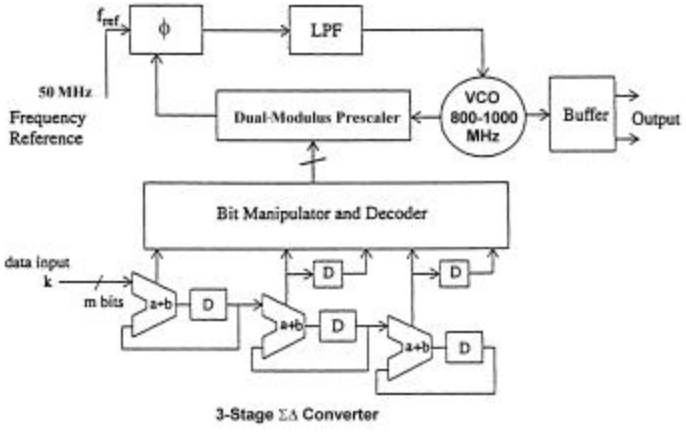

Figure 16 - A block diagram of the fractional-N division synthesizer built using a custom integrated circuit capable of operation at reference frequencies up to 100 MHz. Its use of smaller modulus values is responsible for its frequency extension up to 3 GHz (:4 + :2) with ripple or asynchronous counters, and allows the implementation of dual-modulus counts to M/N+1.

Advanced fractional-N synthesizers not only have a long accumulator, but also a very efficient spurious cancellation mechanism which is based on proprietary mathematical algorithms. This is the area of greatest research and patent application. Our software, which had been developed for the internal fractional division chip, allows programming "software simulation" which will then

be activated in the actual hardware. The screen image of the control software is shown in Figure 17. It accepts all the necessary values. On the top left it gets told the fractional and integer value resulting in an output frequency of 200.007MHz using the 10MHz reference. The correcting mechanism requires the entry of distortion coefficients of the phase detector and algorithm coefficients which can be entered. The values shown correspond to a particular compensation scheme. The display in the left corner shows the equivalent phase noise generated by this internal circuitry. The phase noise at the VCO is shown to be around –130dBc/Hz and then increases at 5E-2, relative to the reference frequency. This means that the loop bandwidth (order of the PLL has to be at least three in order to supress the quantisation noise caused by the digital phase jittering, increases by 60dB/decade, using four accumulators) should be set around this value. The loop filter itself will attenuate the noise on the right side of the picture, where it can be seen that the quantisation noise increases from 50E-2. A Type-2, fourth order filter is used to achieve this. Since the linearity of the phase detector is crutial, the software checks if the chosen coefficients do not overdeviate the phase detector. This is shown in the window on the right. Finally, the distribution of the compensation values also needs to be monitored as it determines overall performance.

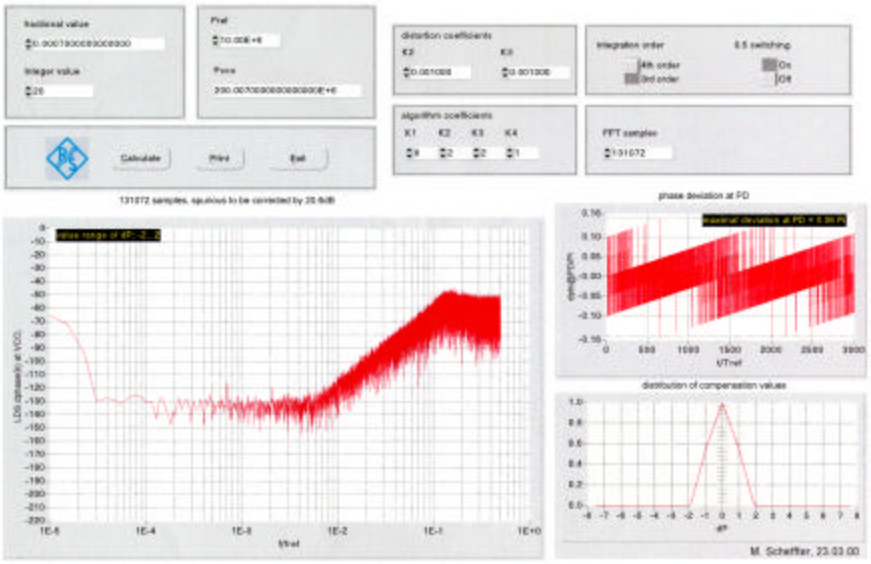

Figure 17 – Simulation of a ΣΔ converter principle of the order of 4. It contains the compensation circuitry for the fractional-N synthesizer.

We now take the systems software again to look at the overall result. The solid curve shows the overall phase noise including unwanted spurious results. Using the coefficients as chosen above, including the loop filter, the ultimate noise floor up to 1.05MHz is better than –140dBc/Hz reaching –180dBc/Hz at 4.5MHz. By “playing” with this coefficients, one can achieve a trade-off between the amplitude of the spurious and the cut-off of the loop. It is also possible to add additional filtering to increase the spurious suppression above 100KHz. In the case shown, the loop bandwidth was set 10KHz. The noise flow of the buffer amplifier following the reference was –165dBc/Hz , and finally, the fractional divider had a noise flow of –150dBc/Hz. The output frequency generated was 200.007MHz. This means that the fractional portion had three digits of resolution.

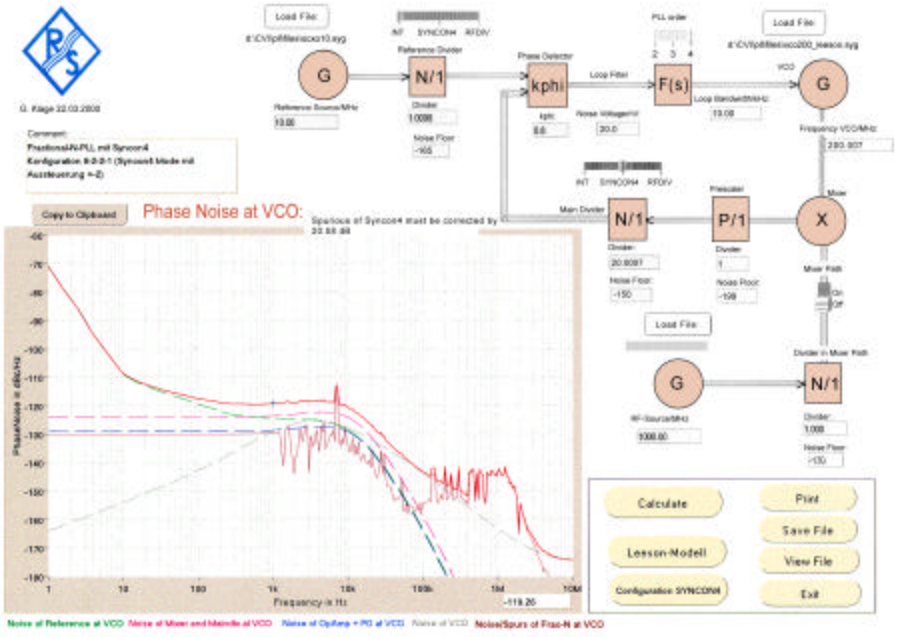

Figure 18 - Composite phase noise of the fractional-N synthesizer system, including all noise and spurious signals generated within the system. The discrete spurious of 7KHz is due to the nonlinearity of the phase detector. Its value needs to be corrected by 20.58dB to a lesser value because of the bandwidth of the FFT analyzer.

SUMMARY

This paper has shown that it is necessary to incorporate the loaded as well as the unloaded Q in all considerations. This necessity resulted in expanding the Leeson equation. The tuning diodes, based on the tuning sensitivity (MHz/V), can add significantly to the phase noise, if not dominated. Since there are various approaches for fractional-N dividers around, we wanted to show what influence the digital portion of the synthesizer chip has on the resulting phase noise of the system. Since we had a compensation circuit with arbitrary digital compensation coefficients, we were able to select a practical case which demonstrates the impact of the various choices. In most cases, the designer is "stuck" with a particular hardware design and rarely gets a fractionality beyond 1/32. Chips which provide higher resolution like the one by Philsar achieve their resolution down to 100Hz with a 200KHz reference at the expense of a minimum division ratio, which is larger than 20 (28 bit resolution). Our chip design provides a 54 bit resolution. In the previous example, the fractional offset of 7KHz was selected to show the resulting spurious. The result is that the fractional offset is inside the loop bandwidth. Standard fractional synthesizers don't face the problem that "channel spacing" is smaller than the loop bandwidth. In these cases, a complicated compensation scheme is necessary, as well as a complete spurious analysis. While most authors only look at the smaller division ratio possibilities of the fractional-N principle, it must not be forgotten that due to finite linearity of the phase detector, the noise floor and the generation of spurious frequencies inside the loop

bandwidth increases. This means that for smaller division ratios, and approaching the limits of linearity of the phase detector, the total noise spectrum can deteriorate. The designer, therefore, needs information regarding the linearity of the phase detector and its frequency dependent noise performance, which, in most cases, the manufacturer does not provide.

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