

INTELLIGENT INTERACTIVE SYNTHESIZER

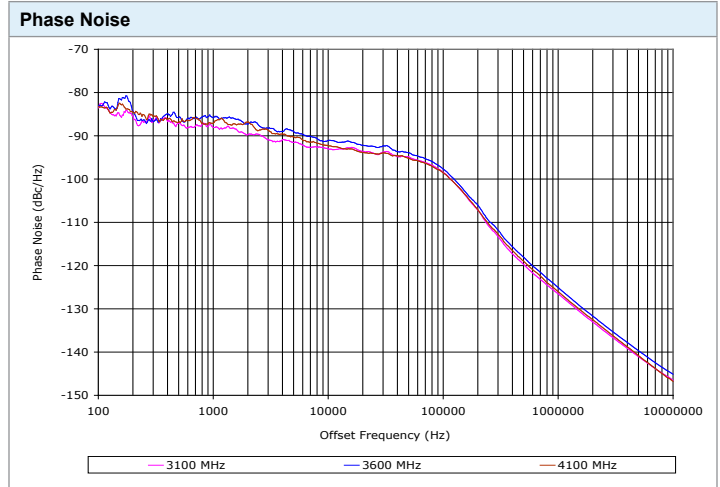
SURFACE MOUNT MODEL: FSH310410-1M

OPTIMIZED LOOP PARAMETER

3100 - 4100 MHz

FEATURES:

- ▶ Exceptionally Low Phase Noise
- ▶ Optimized Reference Sidebands
- ▶ Lead Free - RoHS Compliant
- ▶ Patented REL-PRO® Technology
- ▶ Small Size, Surface Mount
- ▶ Buffered Output

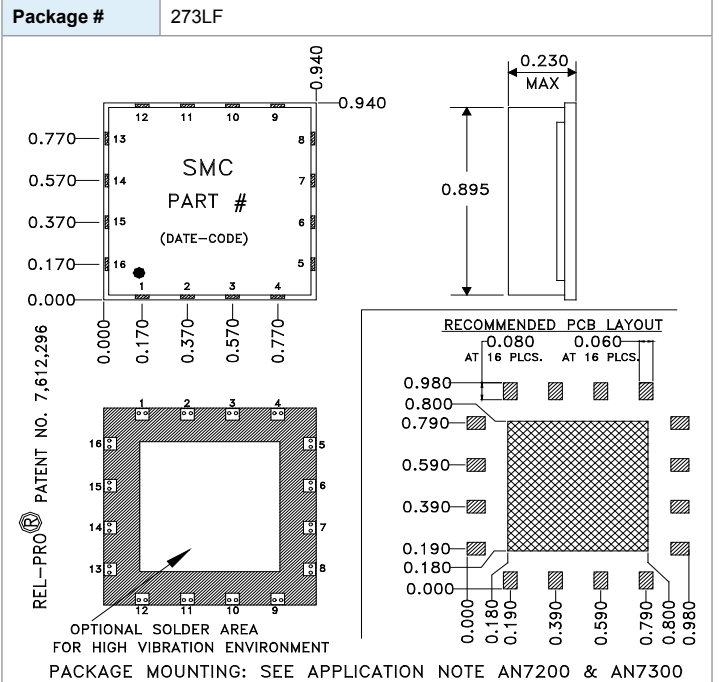


SPECIFICATIONS (Rev. C 04/04/11)

Frequency	3100 - 4100 MHz	
Step Size	10 MHz	
Reference Input Frequency	10 MHz ¹	
Reference Input Voltage	1.0 V p-p to 3.3 V p-p	
Bias Voltage	Vcc	I (mA Max.)
	Digital	+5 15
	VCO	+5 65
	Tune	+12 10
Lock Detect Indicator	CMOS 3.3 V	
Output Power	+5 dBm (Min.)	
Spurious Suppression	75 dB (Typ.)	
Harmonic Suppression	22 dB (Typ.)	
Settling Time	3 mSec (Typ.) ²	
Output Impedance	50 Ohms (Nom.)	
Typical Phase Noise	Offset	Phase Noise
	@ 10 kHz	-92 dBc/Hz
	@ 100 kHz	-98 dBc/Hz
Operating Temperature Range	-40 to +85 °C	
Programming	See Application Note: AN7100	

¹ Reference input frequency is programmable (See AN7100) in multiples of the step size, 10 MHz is the default setting, 150 MHz (Max.)

² From the rising edge of LE to stable lock detect



Absolute Maximum Ratings

Storage Temp. Range	-55 to +125 °C
Bias Voltage (Digital)	+5.25 V
Bias Voltage (Tune)	+16 V
Bias Voltage (VCO)	+5.5 V
DC Voltage Applied to RF Out	±25 V

PORT CONFIGURATION		
Pin 1,2,3 - NC	Pin 8 - Vcc (Tune)	Pin 16 - Clock In
Pin 4 - Error flag	Pin 9 - Vcc (VCO)	All Others - Ground
Pin 5 - Latch Enable In	Pin 13 - RF Out	
Pin 6 - Ref. In	Pin 14 - Lock Detect Out *	NC - No Connection
Pin 7 - Vcc (Digital)	Pin 15 - Data In	

* High when locked (source/sink 500 uA)
 ** A low on this input will reset the internal controller. Leave unconnected for normal operation.

This product is manufactured under one or more of the following patents. Approved: 5,160,810; 5,122,621; 5,390,349; 5,416,449; 5,650,754; 5,805,431; 6,525,623; 6,850,575; 7,088,189; 7,180,381; 7,196,591; 7,262,670; 7,265,642; 7,292,113; 7,365,612; 7,495,525; 2,548,311; 2,548,317; 7,545,229; 7,580,693; 7,586,381; 7,605,670; 7,636,021; 2,533,623
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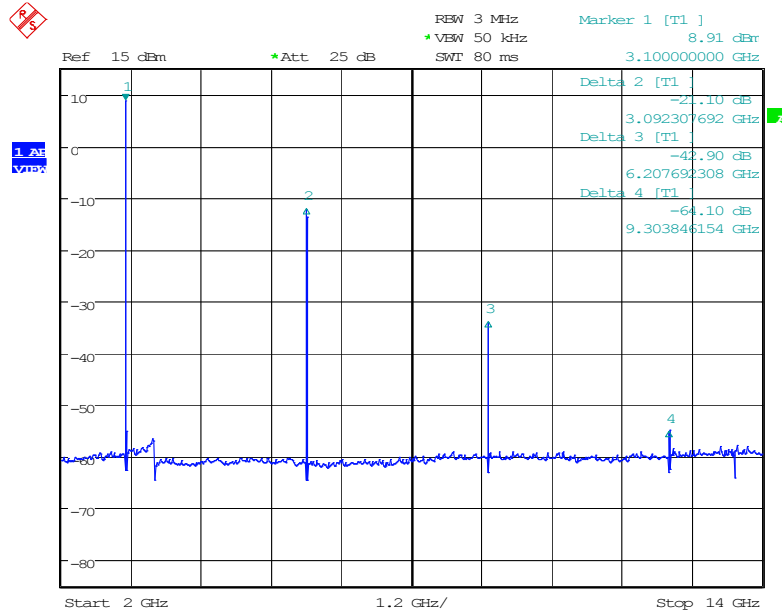
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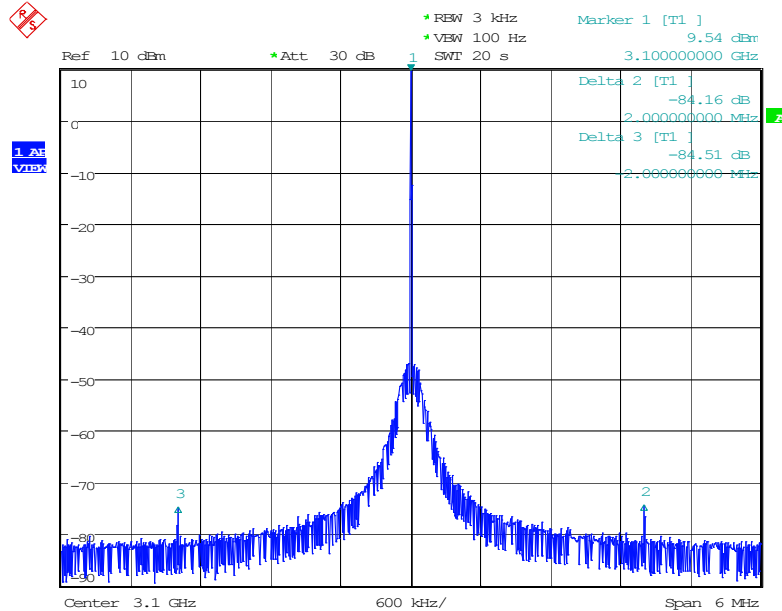
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HARMONIC SUPPRESSION



REFERENCE SIDEBAND SUPPRESSION



PERFORMANCE PLOTS

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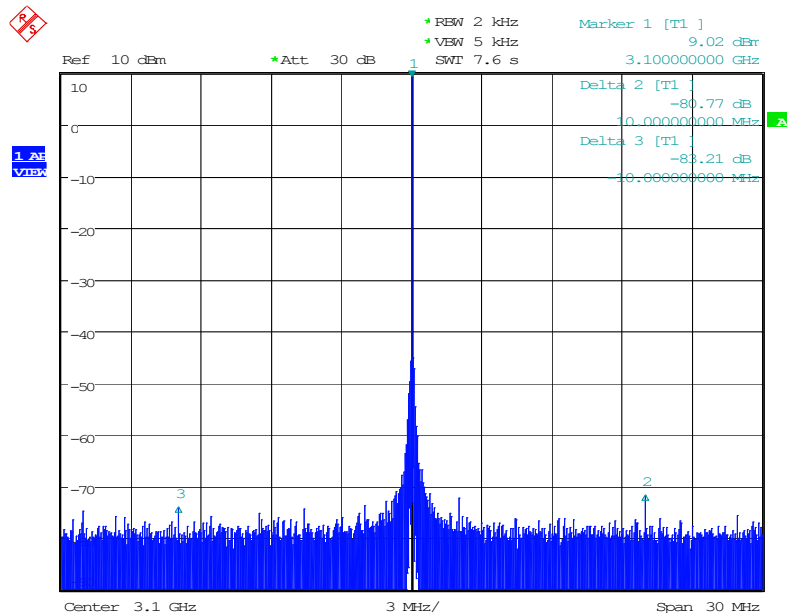
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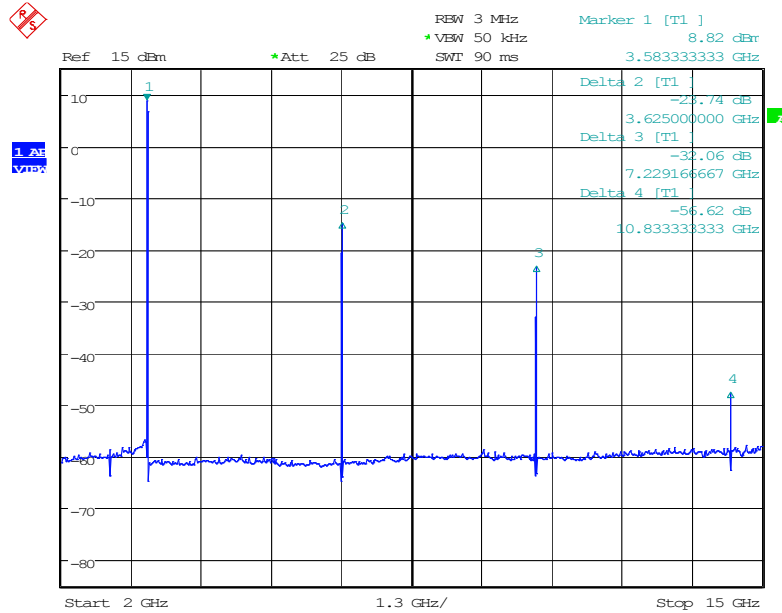
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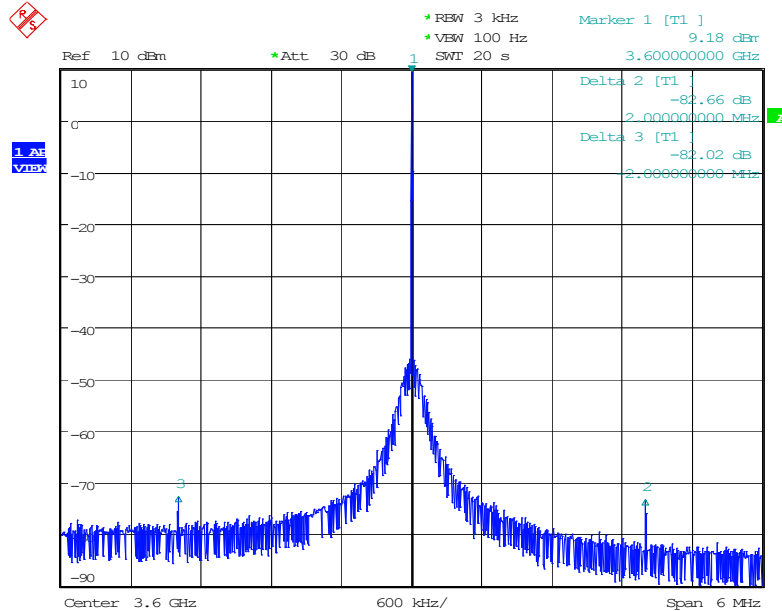
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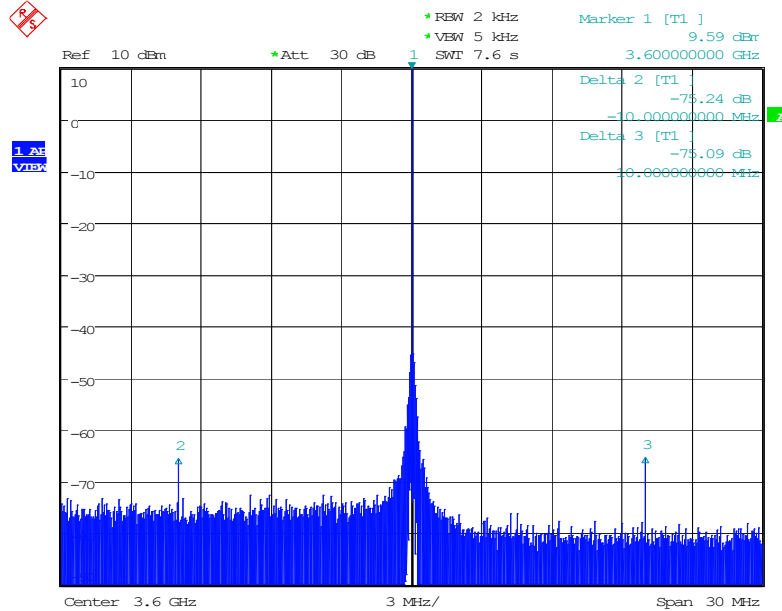
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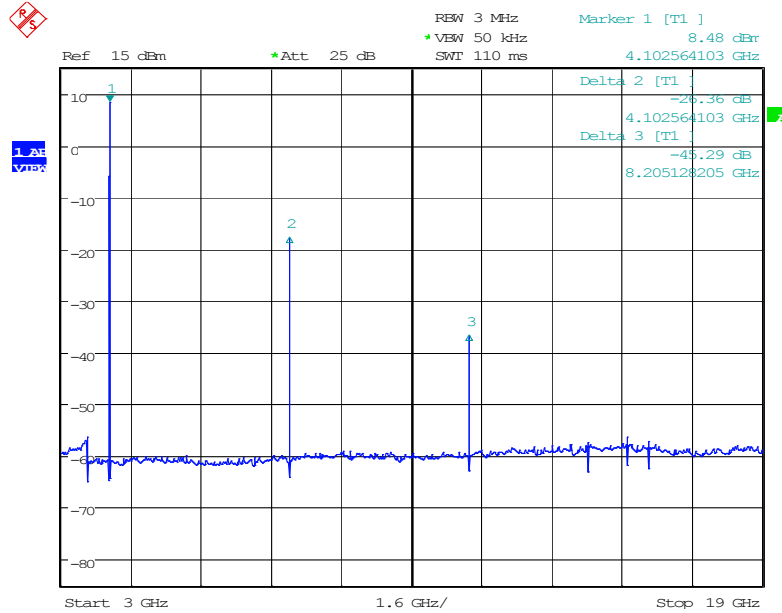
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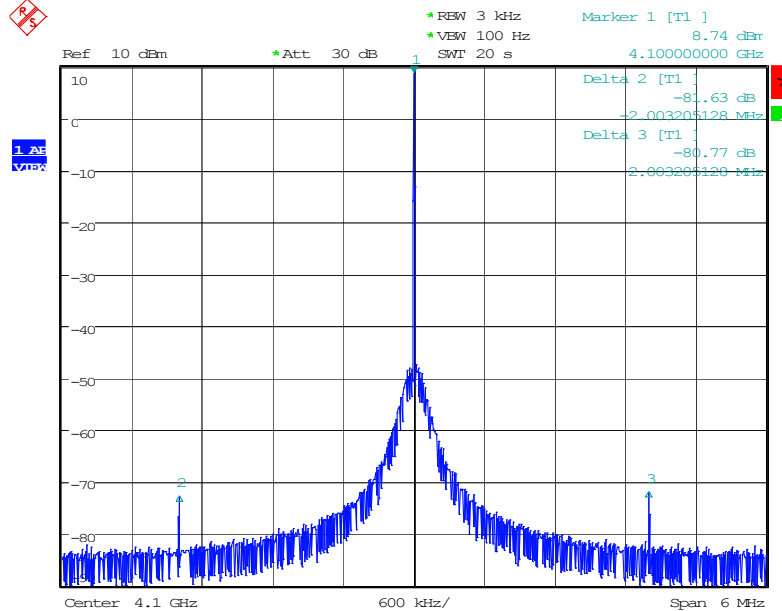
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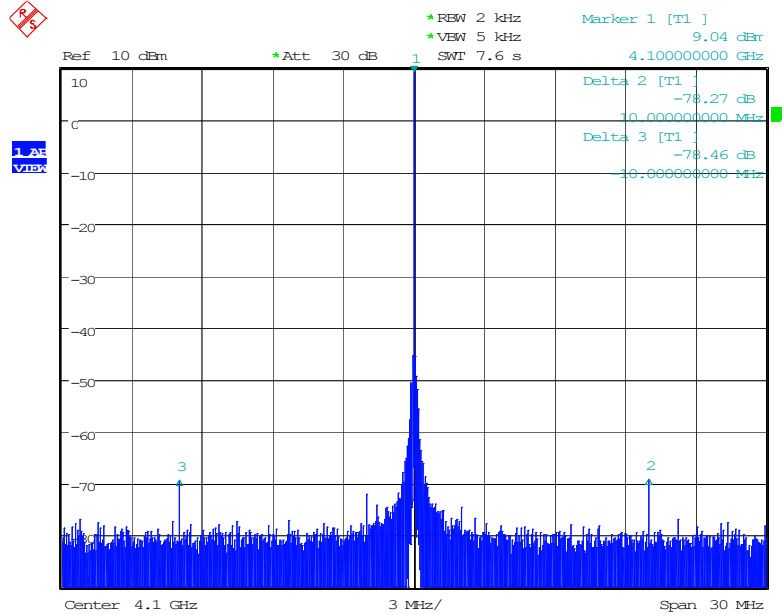
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