

# INTELLIGENT INTERACTIVE SYNTHESIZER

## SURFACE MOUNT MODEL: FSH250300-1M

### OPTIMIZED LOOP PARAMETERS

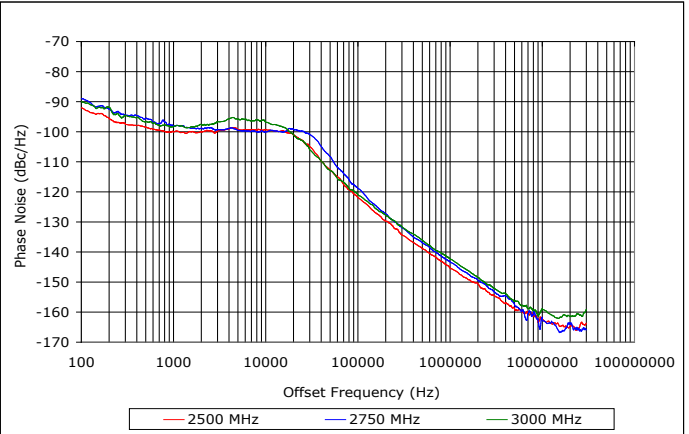
2500 - 3000 MHz

#### FEATURES:

- ▶ Exceptionally Low Phase Noise
- ▶ Optimized Reference Sidebands
- ▶ Lead Free Patented REL-PRO® Technology
- ▶ Small Size, Surface Mount
- ▶ Buffered Output



Phase Noise



#### SPECIFICATIONS (Rev. D 04/29/11)

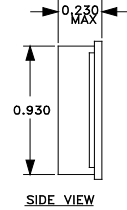
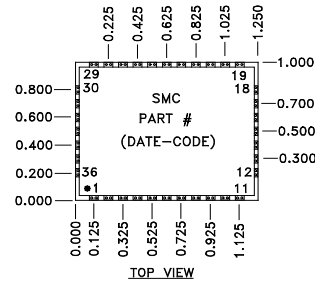
Frequency	2500 - 3000 MHz		
Step Size	10 MHz		
Reference Input Frequency	10 MHz <sup>1</sup>		
Reference Input Voltage	1.0 V p-p to 3.3 V p-p		
Bias Voltage	Vcc	V (Vdc)	I (mA Max.)
	Digital	+5	40
	VCO	+10	35
	Tune	+24	10
Output Power	+6 dBm (Min.)		
Spurious Suppression	100 dB (Typ.)		
Harmonic Suppression	25 dB (Typ.)		
Settling Time	3 mSec (Typ.) <sup>2</sup>		
Output Impedance	50 Ohms (Nom.)		
Lock Detect Indicator	CMOS 3.3 V		
Typical Phase Noise	Offset	Phase Noise	
	@ 1 kHz	-98 dBc/Hz	
	@ 10 kHz	-98 dBc/Hz	
	@ 100 kHz	-120 dBc/Hz	
Operating Temperature Range	-40 to +85 °C		
Programming	See Application Note: AN7100		

<sup>1</sup> Reference input frequency is programmable (See AN7100) in multiples of the step size, 10 MHz is the factory default setting. 150 MHz (Max.)  
<sup>2</sup> From the rising edge of LE to stable lock detect

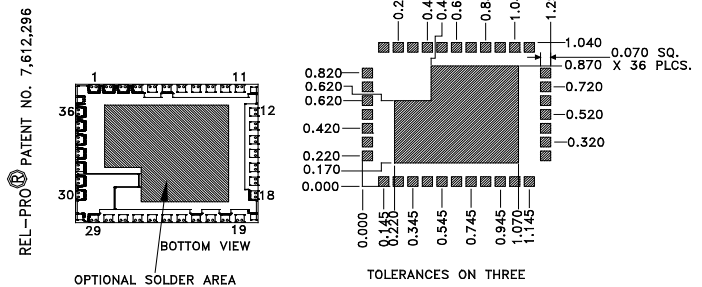
#### Absolute Maximum Ratings

Storage Temp. Range	-55 to +125 °C
Bias Voltage (Digital)	+5.25 V
Bias Voltage (VCO)	+10.5 V
Bias Voltage (Tune)	+26 V
DC Voltage Applied to RF Out	±25 V

Package # 197LF



#### RECOMMENDED PCB LAYOUT



TOLERANCES ON THREE DECIMAL PLACES = ± 0.015

PACKAGE MOUNTING: SEE APPLICATION NOTES AN7200 & AN7300

#### Port Configuration

Pin 5 - RF Out	Pin 19 - Latch Enable In	Pin 8,12,13,14 - NC
Pin 7 - Lock Detect Out *	Pin 21 - Ref. In	Pin 15,17,26,28 - NC
Pin 9 - Data In	Pin 23 - Vcc (Digital)	
Pin 10 - Error Flag	Pin 24 - Vtune Out	All Others - Ground
Pin 11 - Clock In	Pin 25 - Vcc (VCO)	NC - No Connection
Pin 16 - Reset	Pin 27 - Vcc (Tune)	

\* High when locked (source/sink 500 uA)

This product is manufactured under one or more of the following patents. Approved: 5,160,810; 5,122,621; 5,390,349; 5,416,449; 5,650,754; 5,805,431; 6,525,623; 6,850,575; 7,088,189; 7,180,381; 7,196,591; 7,262,670; 7,265,642; 7,292,113; 7,365,612; 7,495,525; 2,548,311; 2,548,317; 7,545,229; 7,580,693; 7,586,381; 7,605,670; 7,636,021; 2,533,623  
 | Pending: 60/493075; 60/501371 & 60/501790; 60/527957 & 60/528670; 60/563481; 60/564173; 60/589090; 60/601823; 60/605791; EV31369834; 11/259766; 60/622485 & 60/710310; 10/937525/60/736901; 60/732787; 7,495,525; 2,548,311; 2,548,317; 7,545,229; 2,563,174; 7,580,693; 7,612,296; 2,524,751

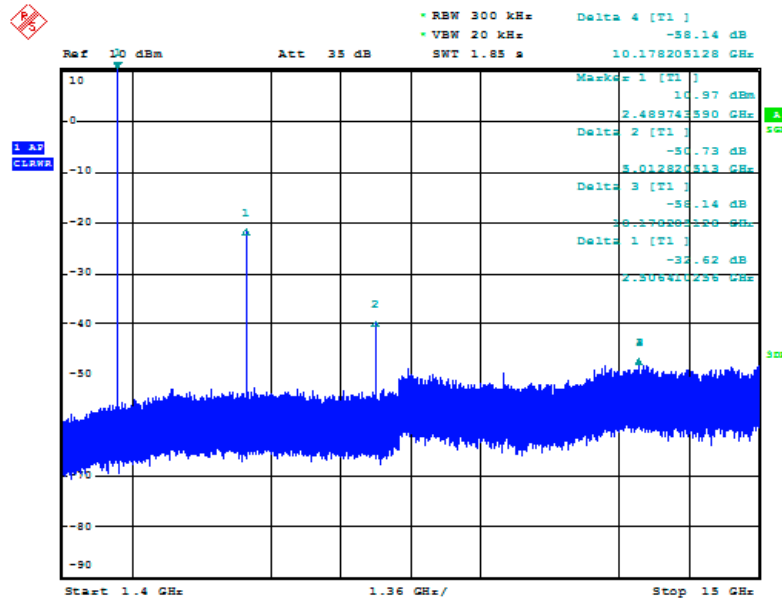
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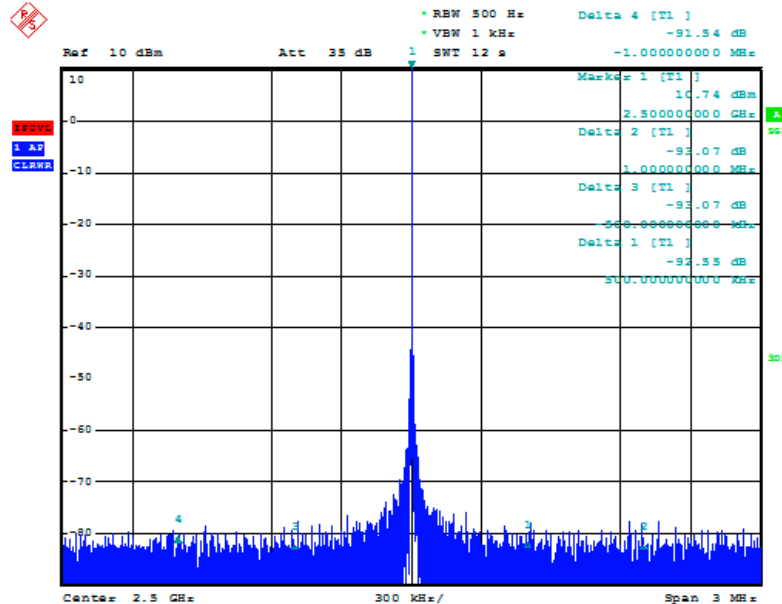
OPTIMIZED LOOP PARAMETERS

2500 - 3000 MHz

### HARMONIC SUPPRESSION



### REFERENCE SIDEBAND SUPPRESSION



PERFORMANCE PLOTS

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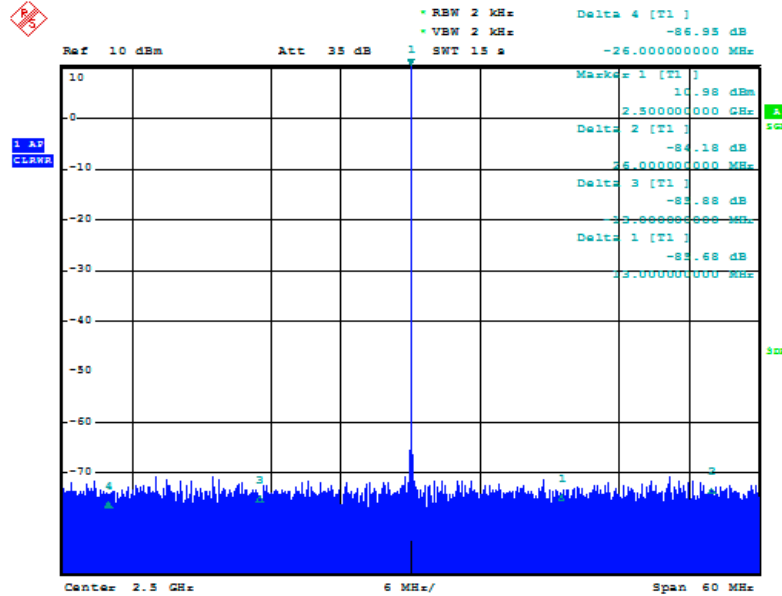
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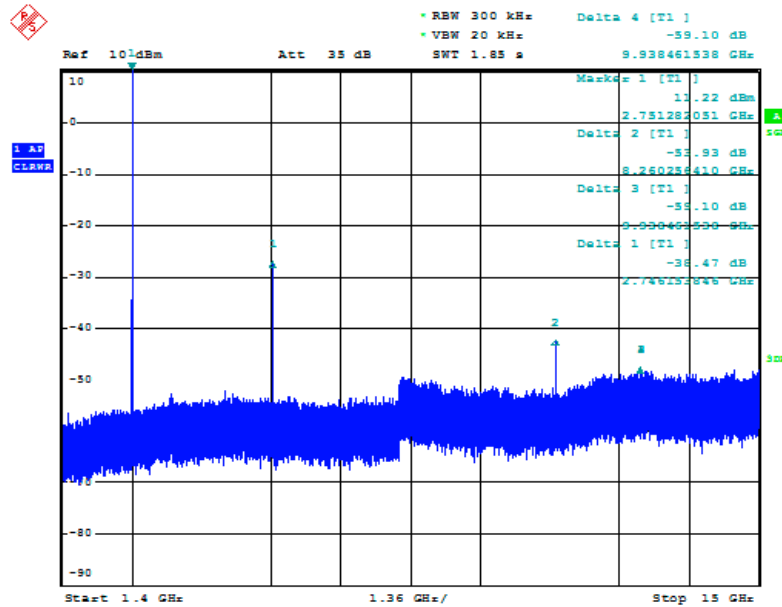
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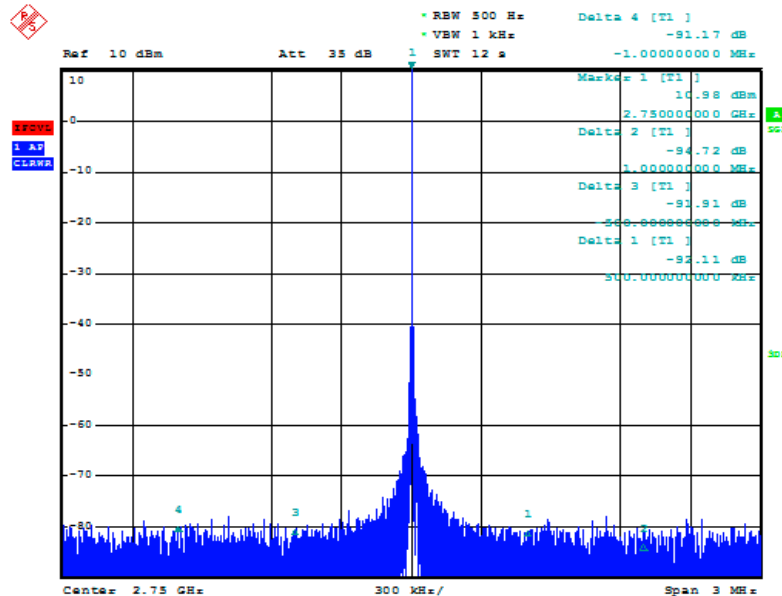
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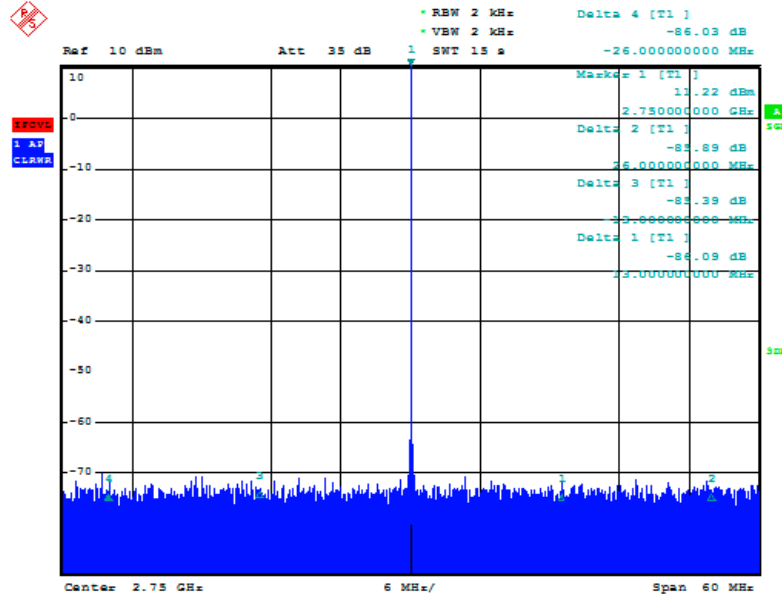
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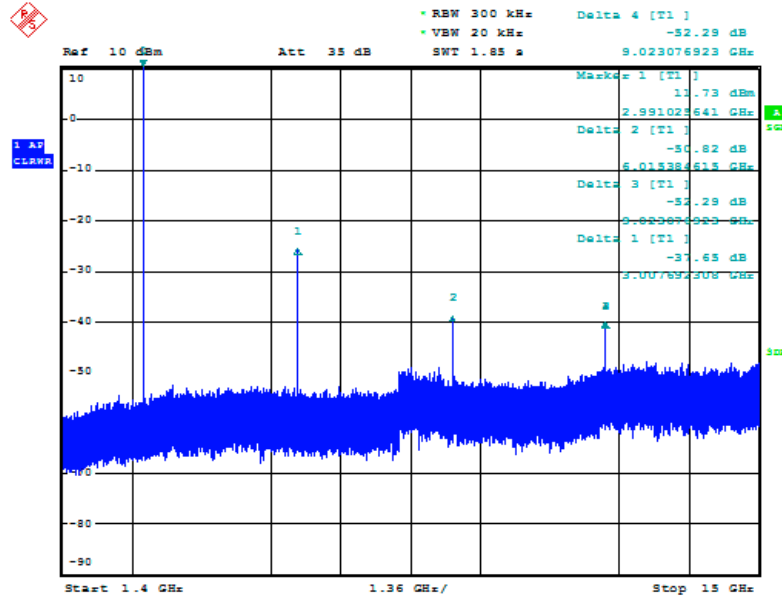
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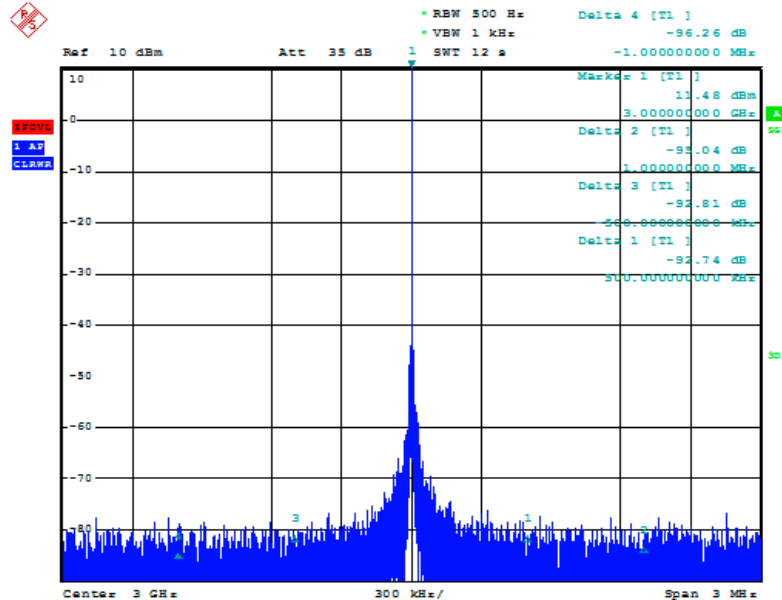
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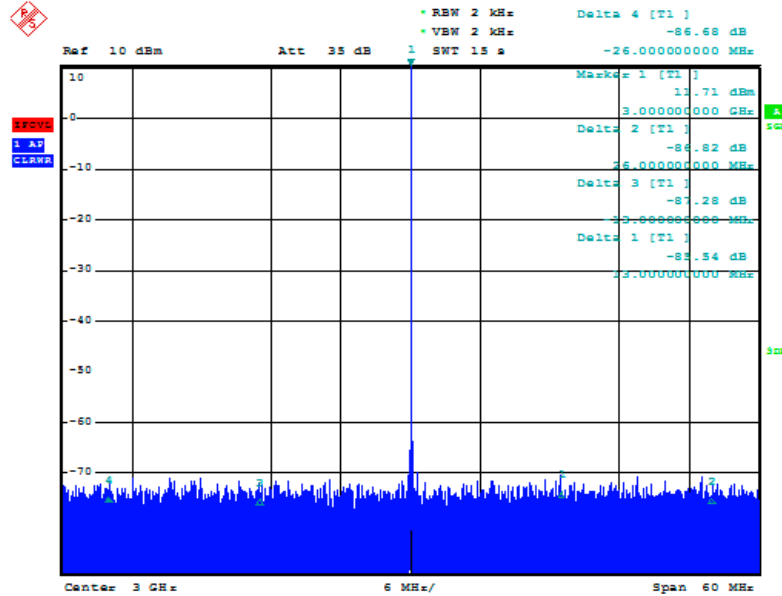
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