

INTELLIGENT INTERACTIVE SYNTHESIZER

SURFACE MOUNT MODEL: LFSW2476-50

WIDE BANDWIDTH

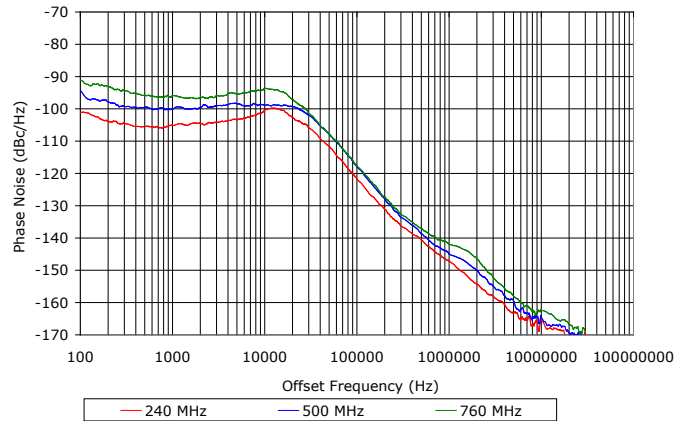
240 - 760 MHz

FEATURES:

- ▶ Exceptionally Low Phase Noise
- ▶ Interactive Communication
- ▶ Standard Programming Interface
- ▶ Ultra Wide Tuning Range
- ▶ Lead Free - RoHS Compliant
- ▶ Patented REL-PRO® Technology
- ▶ Small Size, Surface Mount
- ▶ Buffered Output



Phase Noise

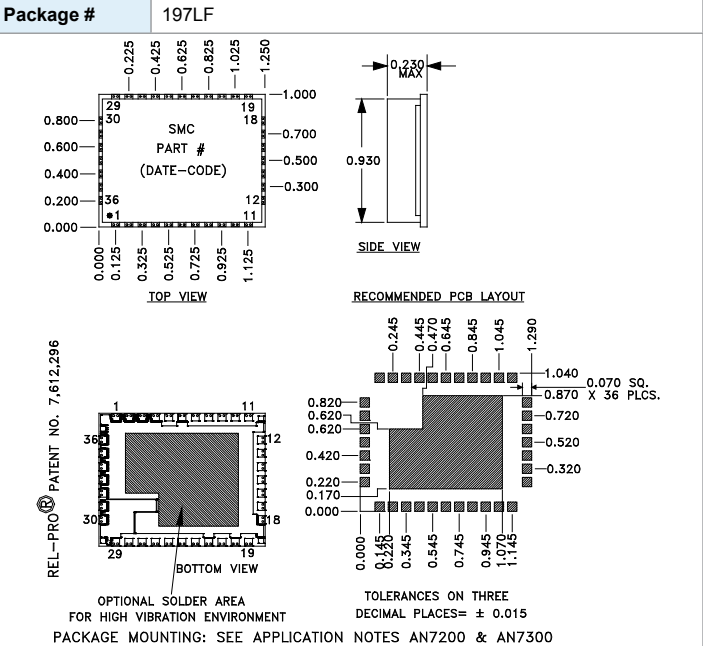


SPECIFICATIONS (Rev. A 06/16/11)

Frequency	240 - 760 MHz		
Step Size	500 kHz		
Reference Input Frequency	10 MHz ¹		
Reference Input Voltage	1 V p-p to 3.3 V p-p		
Bias Voltage	Vcc	V (Vdc)	I (mA Max.)
	Digital	+5	50
	VCO	+5	30
	Converter	+5	60
Lock Detect Indicator	CMOS 3.3 V		
Output Power	+5 dBm (Min.)		
Spurious Suppression	75 dB (Typ.)		
Harmonic Suppression	15 dB (Typ.)		
Settling Time	5 mSec (Typ.) ²		
Output Impedance	50 Ohms (Nom.)		
Typical Phase Noise	Offset	Phase Noise	
	@ 1 kHz	-100 dBc/Hz	
	@ 10 kHz	-100 dBc/Hz	
@ 100 kHz	-119 dBc/Hz		
Operating Temperature Range	-40 to +85 °C		
Programming	See Application Note: AN7100		

¹ Reference input frequency is programmable (See AN7100) in multiples of the step size, 10 MHz is the factory default setting. 100 MHz (Max.)

² From the rising edge of LE to stable lock detect



Absolute Maximum Ratings

Storage Temp. Range	-55 to +125 °C
Bias Voltage (Digital)	+5.25 V
Bias Voltage (VCO)	+5.5 V
Bias Voltage (Converter)	+8 V
DC Voltage Applied to RF Out	±25 V

Port Configuration		
Pin 5 - RF out	Pin 21 - Ref. In	Pin 8,12,14,15,16,17 - NC
Pin 7 - Lock Detect Out *	Pin 23 - Vcc (Digital)	All Others - Ground
Pin 9 - Data In	Pin 24 - Vtune (Output)	
Pin 10 - Error Flag	Pin 25 - Vcc (VCO)	
Pin 11 - Clock In	Pin 26 - Vout (Converter) ***	
Pin 13 - VCO (On/Off)****	Pin 27 - Vcc (Tune) ***	
Pin 19 - Latch Enable In	Pin 28 - Vcc (Converter)	

* High when locked (source/sink 500 uA)

*** Connect externally. Bypassed with a 10uF 35V tantalum capacitor.

**** NC if unused.

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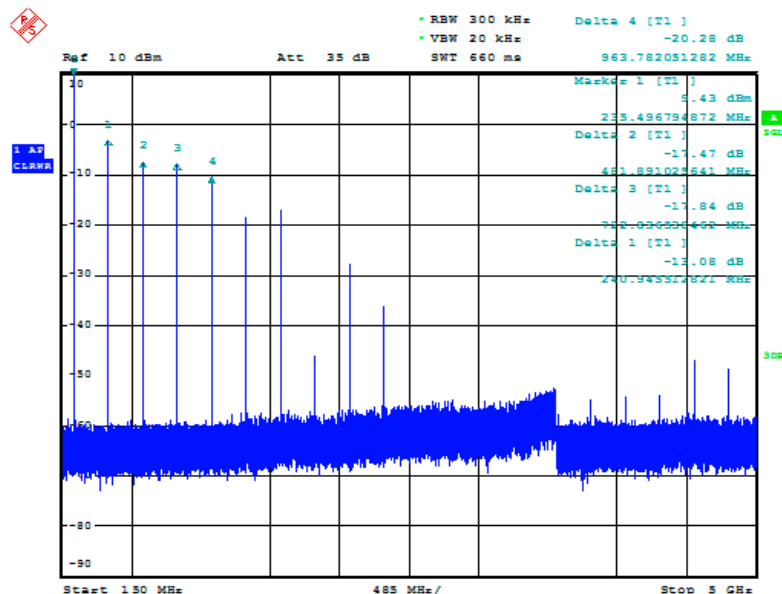
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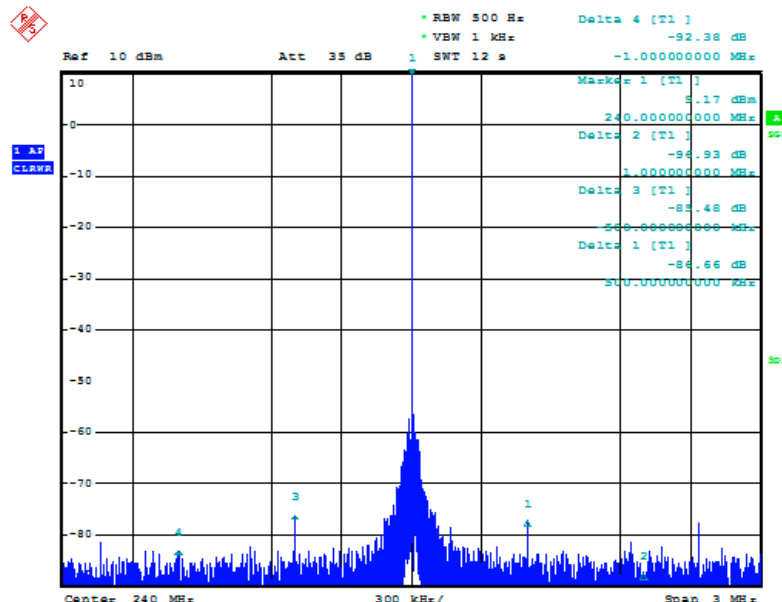
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240 - 760 MHz

HARMONIC SUPPRESSION



REFERENCE SIDEBAND SUPPRESSION



PERFORMANCE PLOTS

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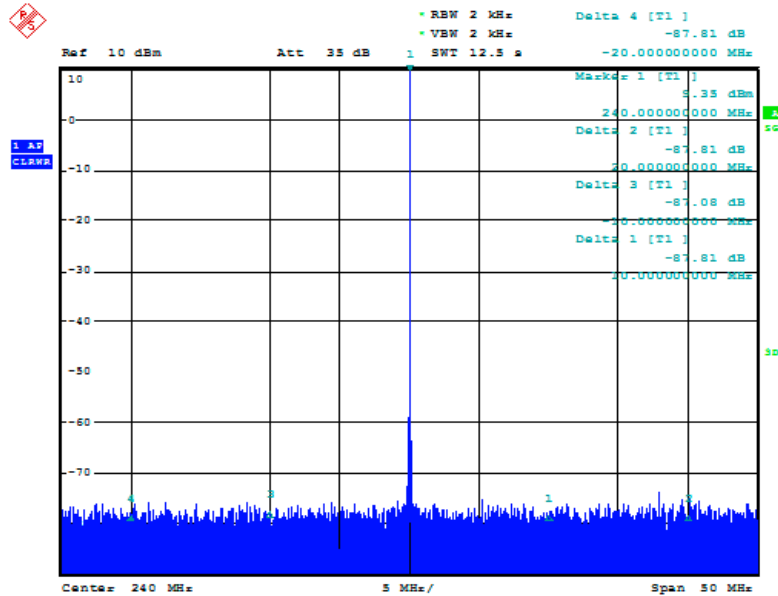
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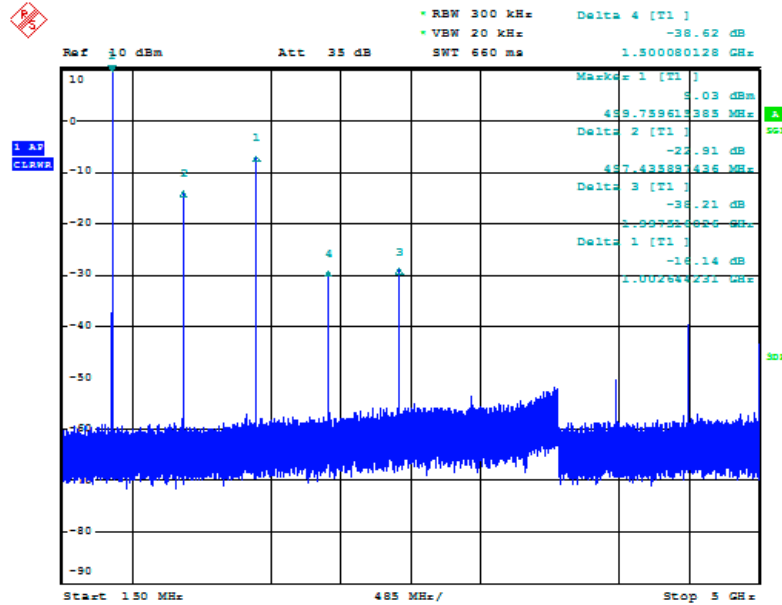
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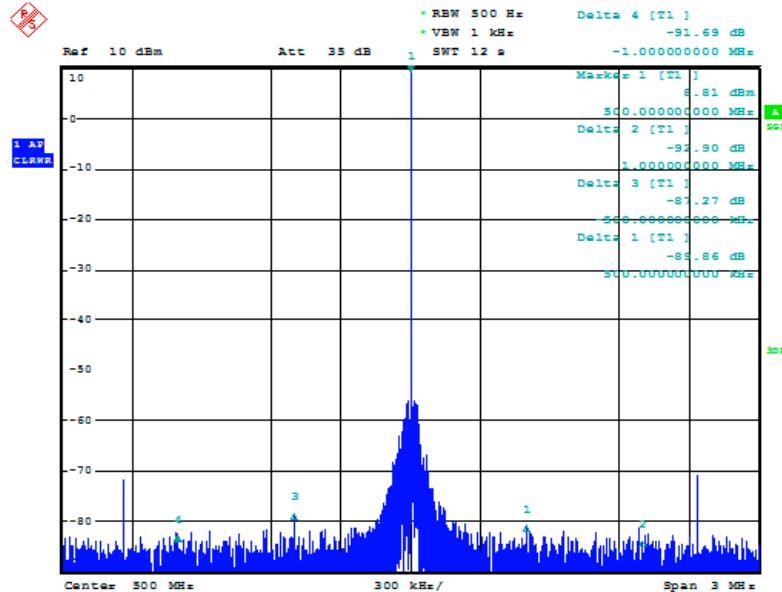
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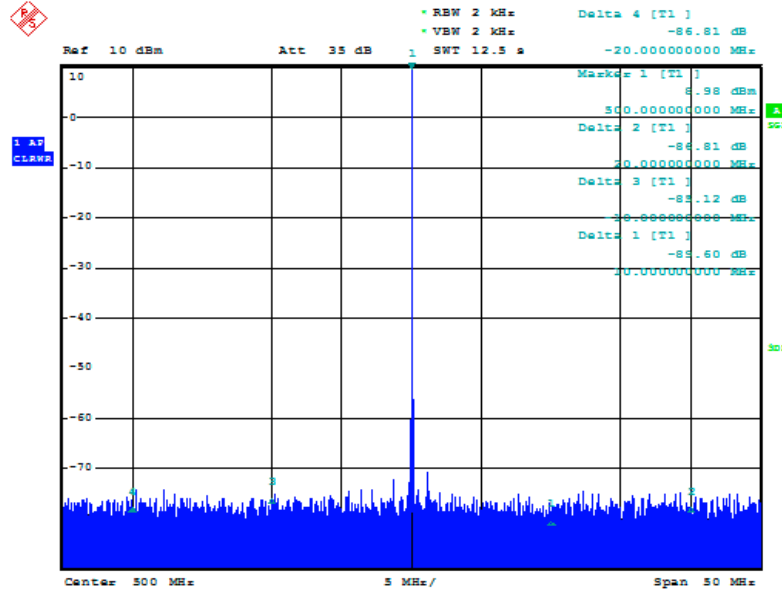
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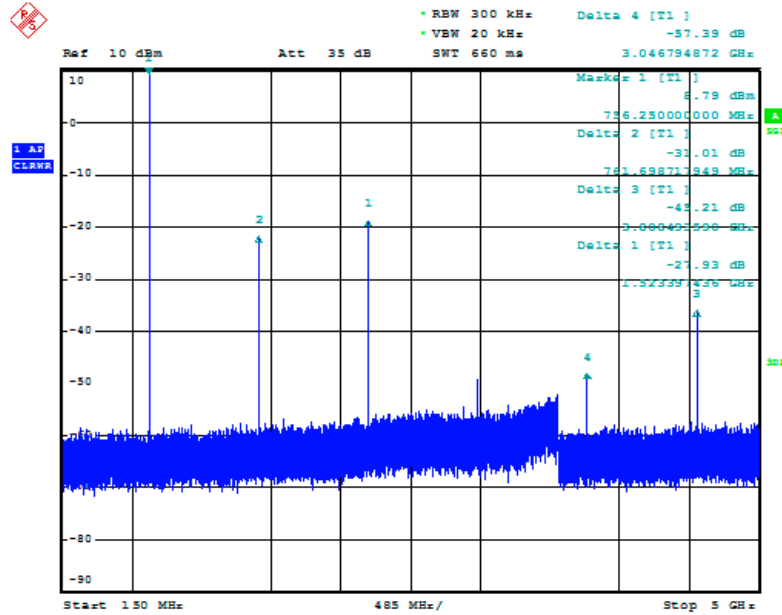
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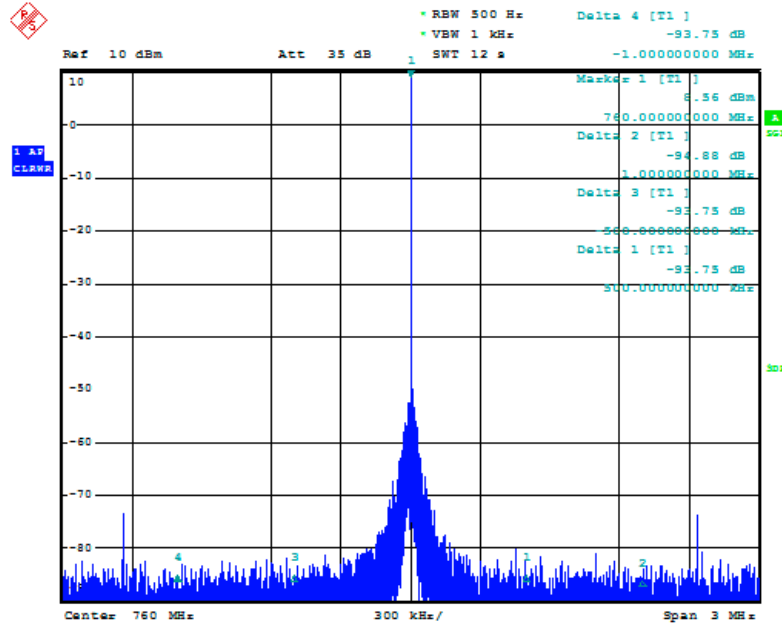
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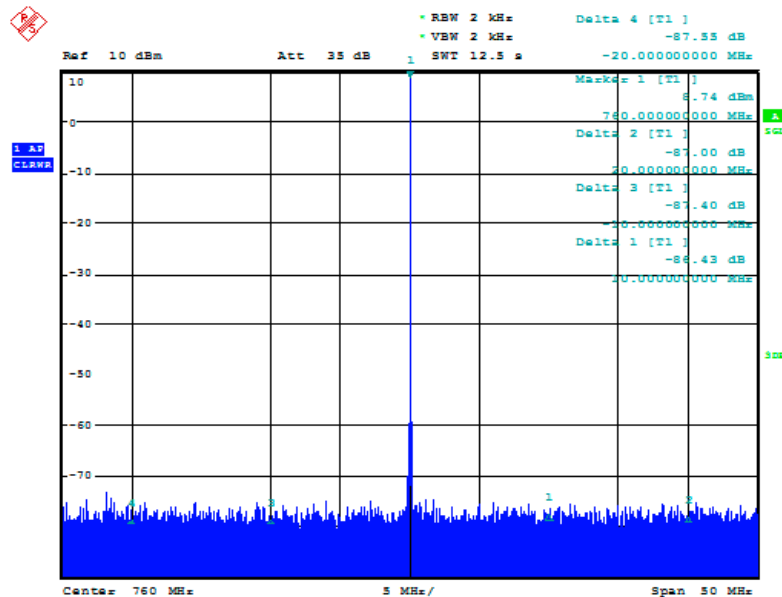
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